TEK
070-6603-00
Product Group 37

2440
OSCILLOSCOPE
SERVICE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

Please Check for CHANGE INFORMATION at the Rear of This Manual

First Printing JUL 1988
Revised JUN 1989

Tektronix®
COMMITTED TO EXCELLENCE

Printed in U.S.A. Specification and price change privileges are reserved.

Instrument Serial Numbers

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000 Tektronix, Inc., Beaverton, Oregon, USA
100000 Tektronix Guernsey, Ltd., Channel Islands
200000 Tektronix United Kingdom, Ltd., London
300000 Sony/Tektronix, Japan
700000 Tektronix Holland, NV, Heerenveen,The Netherlands

TABLE OF CONTENTS

TABLE OF CONTENTS (cont)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont)

Page

LIST OF TABLES

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found. For maximum input voltage see Table 1-1.

Symbols as Marked on Equipment

DANGER — High voltage.

Protective gound (earth) terminal.

ATTENTION — Refer to manual.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before making any connections to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising from Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for the instrument.

Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the instrument parts list. A replacement fuse must meet the type, voltage rating, and current rating specifications for the fuse that it replaces.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this instrument in an atmosphere of explosive gasses.

Do Not Remove Covers or Panels

To avoid personal injury, the instrument covers or panels should only be removed by qualified service personnel. Do not operate the instrument without covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms bwetween the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding connector in the power cord is essential for safe operation.

SPECIFICATION

INTRODUCTION

The TEKTRONIX 2440 Digital Oscilloscope is a portable, dual-channel instrument with a maximum digitizing rate of 500 Megasamples per second. The scope is capable of simultaneous acquisition of Channel 1 and Channel 2 input signals. It has a real-time useful storage bandwidth of 200 MHz for single-event acquisitions, with an equivalent-time bandwidth of 300 MHz when repetitive acquisitions are acquired. Since both channels are acquired simultaneously, the XY display is available to full bandwidth. Options include a Word Recognition Probe, Video signal triggering, Probe Power, and Rackmounting.

The instrument is microprocessor controlled and menu driven, displaying at the top of the screen alphanumeric CRT readouts of the vertical and horizontal scale factors, trigger levels, trigger source, and cursor measurements. Menus, displayed at the bottom of the CRT display, are used by the operator to select the operating mode.

A user makes decisions as to what operation and mode setup the instrument must have to make the measurement wanted and then selects the proper functions using a combination of front-panel buttons and the displayed menu.

Five menu buttons mounted on the CRT bezel are used to make selections from the entry choices displayed. The top line of the menu display usually contains the menu title, and the bottom line labels the buttons with the control functions they select. The selection is made (indicated by an underscoring of the menu label in the display) when the bezel button below the selected function is pressed. The menus, system operating modes, and auxiliary functions are described in Section 5, "Controls, Connectors, and Indicators" of the Operators manual included with this instrument, and the "Getting Acquainted" procedure in Section 1 of that manual familiarizes the user with menu operation.

VERTICAL SYSTEM

The two vertical channels have calibrated deflection factors from 2 mV to 5 V per division in a 1-2-5 sequence of 14 steps. Use of coded probes having attenuation factors of 1X, 10X, 100X, and 1000X extends the minimum sensitivity to 5,000 V per division (with the 1000X probe) and the maximum sensitivity to 200 μV per division (using a 1X probe in SAVE or AVERAGE expanded mode).

VOLTS/DIV readouts are automatically switched to display a correct scale factor when properly coded probes are attached. Each channel can be separately inverted. ADD and MULT are display functions provided by the processor system.

In SAVE mode, the waveforms may be both horizontally and vertically repositioned, expanded horizontally and vertically, added to each other, or multiplied together for either XY or YT displays.

HORIZONTAL SYSTEM

Horizontal display modes of A, A INTEN, and B Delayed are available. The time base has 29 calibrated SEC/DIV settings in a 1-2-5 sequence from 2 ns per division to 5 s per division. An External Clock mode is provided that accepts clocking signals from 1 MHz to 100 MHz.

The B Trace and the intensified zone on the A INTEN Trace may be delayed by time with respect to the A trigger, and a DELAY by EVENTS function permits the A display to be delayed by a selected number of B Trigger events. In the case of DELAY by EVENTS, the B Trigger SOURCE, COUPLING, SLOPE, and LEVEL controls define the nature of the signal needed to produce events triggering. The number of events required to satisfy the

delay may be set from 1 to 65,536, with a resolution of one event. The DELTA DELAY feature produces two independently settable delayed B Traces in DELAY by TIME.

TRIGGER SYSTEM

The trigger system of the scope provides many features for selecting and processing a signal used in triggering the acquisition system. The conventional features of SOURCE selection, Trigger LEVEL control, Trigger SLOPE, Trigger MODE, and CPLG (coupling) include enhancements not normally found in a conventional oscilloscope.

The choices of VERT, CH1 or CH2, EXT1 or EXT2, LINE, and A*B or WORD (16-bit data word recognition) are available as SOURCE selections for triggering A Horizontal Mode acquisitions. These sources for trigger signals provide a wide range of applications involving specialized triggering requirements. Except for A*B (A AND B) and LINE (power-source frequency), the same Trigger SOURCE selections are available for triggering B acquisitions. The selected trigger signal is conditioned by the choice of input CPLG (coupling). These coupling selections are AC, DC, HF REF, LF REJ, and NOISE REJ. LEVEL control provides a settable amplitude (with CRT readout) at which triggering will occur, and SLOPE control determines on which slope of the triggering signal (plus or minus) the acquisition is triggered.

Trigger MODE choices are AUTO LEVEL, AUTO, NORM, and SINGLE SEQ (single sequence), for the A and A INTENSIFIED Modes, and Triggerable After Delay and Runs After Delay, for the B Mode. AUTO LEVEL provides for automatic leveling on the applied trigger signal. AUTO MODE produces an auto trigger in the event a trigger signal is either not received or not within the limits needed to produce a triggering event. When triggering conditions are met, a normal triggered display results. At SEC/DIV settings of 100 ms per division and longer, the AUTO MODE switches to ROLL. In ROLL MODE, the display is continually updated and trigger signals are disregarded.

NORM (normal) trigger MODE requires that all triggering requirements are met before an acquisition will take place. SINGLE SEQ (single sequence) MODE is a variation of the conventional single-shot displays found on many previous oscilloscopes. In SINGLE SEQ, a single complete acquisition is done on all called-up VERTICAL MODES. Since an acquisition depends on the acquisition mode in effect, many of the scope operating features are altered in SINGLE SEQ. A complete description of this mode is discussed in "Controls, Connectors, and Indicators" in Section 5 of the Operators manual.

The user has a choice of trigger points within the acquired waveform record by selecting the amount of pre-trigger data displayed. The trigger location in the record is selectable from a choice of five pretrigger lengths beginning at one-eighth of the record length and increasing to seven-eighths of the record length. A record trigger position is independently selectable for both A and B acquisitions. Additional trigger positions in the record are selectable via the GPIB interface commands.

CURSOR MEASUREMENTS

Time and Voltage cursors are provided for making parametric measurements on the displayed waveforms. Time may be measured either between the cursor positions (DELTA TIME) or between a selected cursor and the trigger point of an acquired waveform (ABSOLUTE). Time cursor readouts are scaled in seconds, degrees, or percentage values. The 1/TIME cursors may be scaled in hertz (Hz), degrees, or percentage.

Voltage cursor measurements on a waveform display can be selected to read either the voltage difference between the cursor positions or the absolute voltage position of a selected cursor with respect to ground. The volts measurement readouts may be scaled in units of volts, decibels (dB), or percent. The Voltage cursors and Time cursors may also be coupled to track together (V@T and SLOPE) and assigned to a particular waveform for ease in making peak-to-peak and slope waveform measurements. The units for V@T may be volts, percent, or dB; SLOPE may have units of slope (VOLTS/SEC), percent (VOLTS/VOLT), or dB.

WAVEFORM ACQUISITION

Waveforms may be acquired in NORMAL, ENVELOPE, or AVG (Average) acquisition modes; the mode chosen depends on the measurement requirements. NORMAL mode continuously acquires and displays successive acquisitions producing a "live" waveform display similar to that seen with an analog oscilloscope. AVG (averaging) mode averages successive acquisitions of a waveform resulting in an improved signal-to-noise ratio of the displayed waveform. Low-amplitude signals masked by noise become easily visible for making measurements and analysis by averaging from 2 to 256 acquisitions for removing uncorrelated noise. ENVELOPE mode saves the

maximum and minimum data-point values over a selected number of acquisitions from 1 to 256 plus CONT (continuous). The display presents a visual image of the amount of change (envelope) that occurs to a waveshape during the accumulated acquisitions. Frequency, phase, amplitude, and position changes are easily identified when acquiring in ENVELOPE mode. The glitch-catching capability of ENVELOPE mode can capture single-event pulses as narrow as 2 ns at the slowest SEC/DIV setting of 5 seconds per division.

For all three acquisition modes, equivalent-time sampling extends the Useful Storage Bandwidth to 300 MHz if the signal is repetitive and REPET mode is turned on. At 50 ns/DIV and faster, randomly-acquired data points (or samples) taken from successive acquisitions of a periodic signal are used to fill the complete record (1024 data points) of the signal waveform display. Depending on the SEC/DIV setting, as few as 10 data points (at 2 ns/DIV) or as many as 512 data points (at 50 ns/DIV) may be obtained on each triggered acquisition. Sampling of successive acquisitions continues until a predetermined number of data points are acquired and any remaining points in the record are determined by interpolating between the acquired points. (The predetermined number includes at least enough data point to meet the Useful Storage Bandwidth of 300 MHz specified for REPET mode.) These interpolated points are replaced by randomly-acquired data points as they become available from successive acquisitions.

Horizontally, the record length of acquired waveforms is 1024 data points (512 max/min pairs in ENVELOPE mode), of which 500 make up a one-screen display (50 data points per division for 10 divisions). The entire record may be viewed by using the Horizontal POSITION control to position any portion of the record within the viewing area.

STORAGE AND I/O

Acquired waveforms may be saved in any of four REF waveform nonvolatile memories. Any or all of the saved reference waveforms may be displayed for comparison with the waveforms being currently acquired. The source and destination of waveforms to be saved may be user designated. Assignment can be made to save either channel 1 or channel 2 (or the results of an addition or multiplication of the two channels) to any REF memory or to move a stored reference from one REF memory to another. Reference waveforms may also be written into a REF memory location via the GPIB interface.

The scope is fully controllable and capable of sending and receiving waveforms via the standard equipped GPIB interface. This feature makes the instrument ideal for making automated measurements in a production or research and development environment that calls for repetitive data taking. Self- calibration and self-diagnostic features built into the scope to aid in fault detection and servicing are also accessible via commands sent from the GPIB controller.

Another standard feature is the "DEVICES" setting for GPIB Interface control. This feature allows the user to output waveforms (and other on-screen information) from the front panel to many printers and plotters that use HP® Graphics Language. In this way, hard copies of acquired waveforms can be obtained without putting the scope into a system controller environment

EXTENDED FEATURES

There are several other features incorporated into this instrument designed to make it more usable, namely, the HELP, Auto Setup, MEASURE, and AutoStep Sequencer features.

HELP: The HELP function can be used to display operational information about any front-panel control. When HELP mode is in effect, manipulating almost any front-panel control causes the scope to display information about that control. When HELP is first invoked, an introduction to HELP is displayed on screen.

Auto Setup: The Auto Setup function is used to automatically setup the scope for a viewable display based on the input signal. The user can specify the waveform characteristic the display is optimized for (front-edge, period, etc.) from a menu displayed upon executing Auto Setup.

MEASURE: MEASURE automatically extracts parameters from signal input to the scope. In the "SNAPSHOT" mode, 20 different waveform parameters are extracted and displayed for a single acquisition. In the continuous extraction mode, up to four parameters are extracted continuously as the instrument continues to acquire.

AutoStep Sequencer (PRGM): With AutoStep, the user can save single front-panel setups or sequences of setups and associated flow control and Input/Output actions for later recall. If MEASURE and/or OUTPUT are saved as part of these setups they can be used for automatic parameter extraction and data printout. 100 to 800 front-panel setups (depending on complexity) can be stored in one or more sequences.

The complete descriptions of these four features are found in Section 5 of the Operators manual included with this instrument.

The following items are standard accessories shipped with the scope instrument:

2	Probe packages
1	Snap-lock accessories pouch
1	Zip-lock accessories pouch
1	Operators manual
1	Programmer's Reference Guide
2	Users Reference Guide
1	Fuse
1	Power cord (installed)
1	Blue plastic CRT filter (installed)
1	Clear plastic CRT filter
1	Front-panel cover

For part numbers and further information about standard accessories and a list of the optional accessories, refer to "Options and Accessories" (Section 7) in this manual. For additional information on accessories and ordering assistance, contact your Tektronix representative or local Tektronix Field Office.

PERFORMANCE CONDITIONS

The following electrical characteristics (Table 1-1) apply when the scope has been calibrated at an ambient temperature between +20°C and +30°C, has had a warmup period of at least 20 minutes and is operating at an ambient temperature between −15°C and +55°C (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

Environmental characteristics are given in Table 1-2. The scope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4. The rackmounted scope meets the vibration and shock requirements of MIL-T-28800C for Type III, Class 5, Style D equipment when mounted using the rackmount rear-support kit supplied with both the 1R Option and the Rackmount Conversion kit.

Mechanical characteristics of the scope are listed in Table 1-3.

Video Option characteristics are given in Table 1-4.

RECOMMENDED ADJUSTMENTS SCHEDULE

For optimum performance to specification, the internal SELF CAL should be done:

1. If the operating temperature is changed by more that 5°C since the last SELF CAL was performed.

2. Immediately before making measurements requiring the highest degree of accuracy.

Table 1-1
Electrical Characteristics

Characteristics	Performance Requirements
ACQUISITION SYSTEM—CHANNEL 1 AND CHANNEL 2	
Resolution	8 bits.[a] Displayed vertically with 25 digitization levels (DL)[b] per division.
Dynamic Range[a]	
SEC/DIV	
100 or slower	−128 to +127 DL's.
50 to 500 ns	−124 to +123 DL's.
200 ns	−121 to +120 DL's.
100 ns	−113 to +112 DL's.
50 ns to 2 ns	
Repet OFF	−113 to +112 DL's.
Repet ON	121 to 120 DL's.
Record Length	1024 samples.[a] Displayed horizontally with 50 samples per division, 20.48-division trace length.[a]
Sample Rate	10 samples per second to 500 megasamples per second (5 s per division to 100 ns per division).
Sensitivity	
Range	80 μV per DL to 0.2 V per DL in a 1-2-5 sequence of 11 steps (2 mV per division to 5 V per division).
Accuracy	
Normal and Average Modes	Within ±(2% + 1 DL) at any VOLTS/DIV setting for a signal 1 kHz or less contained within ±75 DL (±3 divisions) of center when a SELF CAL has been performed within ±15°C of the operating temperature. Measured on a four- or five-division signal with VOLTS or V@T cursors; UNITS set to delta volts.
Envelope Mode	Add 1% to Normal Mode specifications.
Variable Range	Continuously variable between VOLTS/DIV settings. Extends sensitivity to 0.5 V per DL or greater, 12.5 V per division or greater.

[a]Performance Requirement not checked in the manual.

[b]"DL" is the abbreviation for "digitization level." A DL is the smallest voltage level change that can be resolved by the internal 8-bit A-D converter, with the input scaled to the VOLTS/DIV setting of the channel used. Expressed as a voltage, a DL is equal to 1/25 of a division times the VOLTS/DIV setting.

Table 1-1 (cont)

Characteristics	Performance Requirements
ACQUISITION SYSTEM—CHANNEL 1 AND CHANNEL 2 (cont)	
Bandwidth	Bandwidth is measured with a leveled, low distortion, 50-Ω source, sine-wave generator, terminated in 50 Ω. The reference signal is set to 6 divisions or to the maximum leveled amplitude obtainable if the Volt/Div setting is too high to yield 6 div's on screen. Bandwidth with probe is checked using a probe-tip-to-GR termination adaptor (017-0520-00). Bandwidth with external termination is checked using a BNC 50-Ω feed-through terminator (011-0049-01).
−3 dB Bandwidth	
Normal or Average Modes. Envelope Mode at SEC/DIV settings of 0.2 μs or faster.	Using standard accessory probe or internal termination (not checked with probe in manual).
−15°C to +30°C	Dc to 300 MHz.
+30°C to +55°C	Upper Bandwidth Limit reduced by 2.5 MHz for each °C above 30°C.[a]
Envelope Mode at SEC/DIV settings of 0.5 μs or slower.	Dc to 150 MHz using standard accessory probe, internal 50-Ω termination, or external 50-Ω termination on 1-MΩ input.[a]
−4.7 dB Bandwidth	
Normal or Average Mode. Envelope Mode at SEC/DIV settings of 0.2 μs or faster.	Using 50-Ω external termination on 1-MΩ input.
+30°C to +55°C	Upper Bandwidth Limit reduced by 2.5 MHz for each °C above 30°C.[a]
Single Event Useful Storage Bandwidth	
Normal or Average Mode, SEC/DIV at 0.1 μs or Faster; Repet OFF	DC to 200 MHz (calculated). $USB = \frac{F_{(\text{sample freq max})^c}}{2.5}$
AC Coupled Lower −3 dB Point	
1X Probe	10 Hz or less.[a]
10X Probe	1 Hz or less.[a]
Step Response, Repet and Average On; Average Set to 16	
Rise Time	1.17 ns or less (calculated).[a] $T_r \text{ (in ns)} = \frac{350}{\text{BW (in MHz)}}$

[a]Performance Requirement not checked in the manual.

[c]Sample freq. max. is 500 MHz.

Table 1-1 (cont)

Characteristics	Performance Requirements
ACQUISITION SYSTEM—CHANNEL 1 AND CHANNEL 2 (cont)	
Envelope Mode Pulse Response	
Minimum Single Pulse Width for 50% or Greater Amplitude Capture at 85% or Greater Confidence	2 ns.[a]
Minimum Single Pulse Width for Guaranteed 50% or Greater Amplitude Capture	8 ns.[a]
Channel Isolation	Measured with a 10-division, sine-wave input and equal VOLT/DIV settings on both channels. 100:1 or greater at 100 MHz for VOLT/DIV settings from 2 mV/DIV and 500 mV/DIV; 50:1 or greater at 300 MHz for VOLT/DIV settings from 20 mV/DIV to 500 mV/DIV. 25:1 or greater at 300 MHz for VOLT/DIV settings of 5 mV/DIV and 10 mV/DIV.
Acquired Channel 2 Signal Delay with Respect to Channel 1 Signal at Full Bandwidth	±250 ps.[a]
Input R and C (1 MΩ)	
Resistance	1 MΩ ±0.5%.[a] In each attenuator, the input resistance of all VOLTS/DIV positions is matched to within 0.5%.[a]
Capacitance	15 pF ±2 pF.[a] In each attenuator, the input capacitance of all VOLTS/DIV positions is matched to within 0.5 pF.[a]
Input R (50 Ω)	
Resistance	50 Ω ±1%.[a]
VSWR (DC to 300 MHz)	1.3:1 or better.[a]
Maximum Input Voltage ⚠	5 V rms; 0.5 W·sec for any one-second interval for instantaneous voltages from 5 V to 50 V.

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
ACQUISITION SYSTEM—CHANNEL 1 AND CHANNEL 2 (cont)	
Maximum Input Voltages ⚠	
Input Coupling Set to DC, AC, or GND	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
Common-Mode Rejection Ratio (CMRR); ADD Mode with Either Channel Inverted	At least 10:1 at 50 MHz for common-mode signals of 10 divisions or less with VARIABLE VOLTS/DIV adjusted for best CMRR at 50 kHz.
POSITION	
Range	± (9.3 to 10.4) div., at 50 mV per division with INVERT off, when Self Cal has been done within ±5°C of the operating temperature.
Gain Match between NORMAL and SAVE	±3 DLs for positions within ±5 divisions from center.
Low-Frequency Linearity	
Normal or Average Mode	3 DLs or less compression or expansion of a two-division, center-screen signal when positioned anywhere within the acquisition window.
20-MHz Bandwidth Limiter	
—3 dB Bandwidth	13 MHz to 24 MHz.
100-MHz Bandwidth Limiter	
—3 dB Bandwidth	80 MHz to 120 MHz.
Rise Time	2.9 ns to 4.4 ns.[a]
	With a five-division, fast-rise step (rise time of 300 ps or less) using 50-Ω dc input coupling and VOLTS/DIV setting of 10 mV.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TRIGGERING—A and B	
Minimum P-P Signal Amplitude for Stable[a] Triggering from Channel 1, Channel 2, or ADD Source	
A Trigger	
DC Coupled	0.35 division from DC to 50 MHz, increasing to 1.0 division at 300 MHz; 1.5 divisions at 300 MHz in ADD mode.
NOISE REJ Coupled	1.2 divisions or less from DC to 50 MHz; increasing to 3 divisions at 300 MHz; 4.5 divisions at 300 MHz in ADD mode.
AC Coupled	0.35 division from 60 Hz to 50 MHz; increasing to 1.0 division at 300 MHz; 1.5 divisions at 300 MHz in ADD mode. Attenuates signals below 60 Hz.
HF REJ Coupled	0.50 division from DC to 30 kHz. Attenuates signals above 30 kHz.
LF REJ Coupled	0.50 division from 80 kHz to 50 MHz; increasing to 1.0 division at 300 MHz; 1.5 divisions at 300 MHz in ADD mode. Attenuates signal below 80 kHz.
B Trigger	Multiply all A Trigger specifications by two.
A.B Selected	Multiply all A Trigger specifications by two.
Minimum P-P Signal Amplitude for Stable Triggering[a] from EXT TRIG 1 or EXT TRIG 2 Source	
A Trigger	
EXT Gain = 1	
DC Coupled	17.5 mV from DC to 50 MHz, increasing to 50 mV at 300 MHz.
NOISE REJ Coupled	60 mV or less from DC to 50 MHz; increasing to 150 mV at 300 MHz.
AC Coupled	17.5 mV from 60 Hz to 50 MHz; increasing to 50 mV at 300 MHz. Attenuates signals below 60 Hz.
HF REJ Coupled	25 mV from DC to 30 kHz.
LF REJ Coupled	25 mV from 80 kHz to 50 MHz; increasing to 50 mV at 300 MHz.
EXT Gain = ÷5	Amplitudes are five times those specified for Ext Gain = 1.
B Trigger	Multiply all A Trigger amplitude specifications by two.
A.B Selected	Multiply all A Trigger amplitude specifications by two.

[a]A stable trigger is one that results in a uniform, regular display triggered on the selected slope (±). A stably-triggered display should NOT have the trigger point switch between opposite slopes on the waveform, nor should it "roll" across the screen, as successive acquisitions occur. At TIME/DIV settings of 2 ms/DIV and faster, the TRIG'D LED is constantly lit if the display is stably triggered (the LED can flash for SEC/DIV settings of 10 ms/DIV and slower).

Table 1-1 (cont)

Characteristics	Performance Requirements
TRIGGERING—A and B (cont)	
Maximum P-P Signal Rejected by NOISE REJ Coupling Signals within the Vertical Bandwidth	
Channel 1 or Channel 2 Source	0.4 division or greater for VOLTS/DIV settings of 10 mV and higher. Maximum noise rejected is reduced at 2 mV per division and 5 mV per division.
EXT TRIG 1 or EXT TRIG 2 Source	20 mV or greater when Ext Trig Gain = 1. 100 mV or greater when Ext Trig Gain = ÷5.
EXT TRIG 1 and EXT TRIG 2 Inputs	
Resistance	1 MΩ ±1%.[a]
Capacitance	15 pF ±3 pF.[a]
Maximum Input Voltage ⚠	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
LEVEL Control Range	
Channel 1 or Channel 2 Source	±18 divisions × VOLTS/DIV setting.[a]
EXT TRIG 1 or EXT TRIG 2 Source	
EXT GAIN = 1	±0.9 volt.[a]
EXT GAIN = ÷5	±4.5 volts.[a]
LEVEL Readout Accuracy (for triggering signals with transition times greater than 20 ns)	
Channel 1 or Channel 2 Source	
DC Coupled	
+15°C to +35°C	Within ± [3% of setting + 3% of p-p signal + (0.2 division × VOLTS/DIV setting) + 0.5 mV + (0.5 mV × probe attenuation factor)].
−15°C to +55°C (excluding +15°C to +35°C)	Add (1.5 mV × probe attenuation) to +15°C to +35°C specification.[a]
NOISE REJ Coupled	Add ± (0.6 division × VOLTS/DIV setting) to DC Coupled specifications. Checked at 50 mV per division.

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements		
TRIGGERING—A and B (cont)			
LEVEL Readout Accuracy (for triggering signals with transition times greater than 20 ns)			
(continued)			
EXT TRIG 1 or EXT TRIG 2 Source			
EXT GAIN = 1			
DC Coupled	Within ± [3% of setting + 4% of p-p signal + 10 mV + (0.5 mV × probe attenuation factor)].		
NOISE REJ Coupled	Add ±30 mV to DC Coupled specifications.		
EXT GAIN = ÷5			
DC Coupled	Within ± [3% of setting + 4% of p-p signal + 50 mv + (0.5 mV × probe attenuation factor)].		
NOISE REJ Coupled	Add ±150 mV to DC Coupled specifications.		
Variable A Trigger Holdoff	**A SEC/DIV[a]**	**MIN HO[a]**	**MAX HO[a]**
	2 ns 5 ns 10 ns 20 ns 50 ns 100 ns 200 ns	2-4 μs	9-15 μs

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements		
TRIGGERING—A and B (cont)			
Variable A Trigger Holdoff	**A SEC/DIV[a]**	**MIN HO[a]**	**MAX HO[a]**
	500 ns	5-10 μs	
	1 μs 2 μs 5 μs	10-20 μs 20-40 μs 50-100 μs	100-150 μs
	10 μs 20 μs 50 μs	0.1-0.2 ms 0.2-0.4 ms 0.5-1.0 ms	1-1.5 ms
	100 μs 200 μs 500 μs	1-2 ms 2-4 ms 5-10 ms	10-15 ms
	1 ms 2 ms 5 ms	10-20 ms 20-40 ms 50-100 ms	90-150 ms
	10 ms 20 ms 50 ms	0.1-0.2 s 0.2-0.4 s 0.5-1.0 s	0.9-1.5 s
	100 ms 200 ms	1-2 s 2-4 s	9-15 s
	500 ms 1 s 2 s 5 s	5-10 s	
SLOPE Selection	Conforms to trigger-source and ac-power-source waveforms.		
Trigger Position Jitter (P-P)	Checked in NORMAL ACQUIRE mode with a 5-division step having less than or equal to 1 ns rise time.		
A Mode, B Mode (TRIG AFTER)			
SEC/DIV 100 ns and slower	0.04 x SEC/DIV setting[a,b]		
SEC/DIV 50 ns and faster	(0.04 x SEC/DIV setting) + 200 ps[a,b]		
B Mode (RUNS AFTER)			
SEC/DIV 50 ns and faster	(0.04 x B SEC/DIV + 200 ps[a]		
SEC/DIV 50 μs to 100 ns	0.04 x B SEC/DIV[a]		
SEC/DIV 100 μs and slower	0.08 x B SEC/DIV[a]		

[a]Performance Requirements not checked in the manual.

[b]Use B SEC/DIV setting if mode is B; otherwise, use A SEC/DIV setting.

Table 1-1 (cont)

Characteristics	Performance Requirements
TIME BASE	
Sample Rate Accuracy Average Over 100 or More Samples	±0.0015%.[a]
External Clock Repetition Rate Minimum	1 MHz.[a]
Maximum	100 MHz.[a]
Events Count	1 to 65,536[a]
Events Maximum Repetition Rate	100 MHz.[a]
Signal Levels Required for EXT Clock or EVENTS Channel 1 or Channel 2 SOURCE DC Coupled	0.7 division from DC to 50 MHz; increasing to 2.0 divisions at 100 MHz; 3.0 divisions at 100 MHz in ADD mode.[a]
NOISE REJ Coupled	2.4 divisions or less from DC to 50 MHz; increasing to 6.0 divisions at 100 MHz; 9.0 divisions at 100 MHz in ADD mode.[a]
AC Coupled	0.7 division from 60 Hz to 50 MHz; increasing to 2.0 divisions at 100 MHz; 3.0 divisions at 100 MHz in ADD mode. Attenuates signals below 60 Hz.[a]
HF REJ Coupled	1.0 division from DC to 30 kHz. Attenuates signals above 30 kHz.[a]
LF REJ Coupled	1.0 division from 80 kHz to 50 MHz; increasing to 2.0 divisions at 100 MHz; 3.0 divisions at 100 MHz in ADD mode. Attenuates signals below 80 kHz.[a]
EXT TRIG 1 or EXT TRIG 2 Source Ext Gain = 1 DC Coupled	35 mV from DC to 50 MHz; increasing to 100 mV at 100 MHz.[a]
NOISE REJ Coupled	120 mV or less from DC to 50 MHz; increasing to 300 mV at 100 MHz.[a]
AC Coupled	35 mV from 60 Hz to 50 MHz; increasing to 100 mV at 100 MHz. Attenuates signals below 60 Hz.[a]
HF REJ Coupled	50 mV from DC to 30 kHz.[a]
LF REJ Coupled	50 mV from 80 kHz to 50 MHz; increasing to 100 mV at 100 MHz.[a]
Ext Gain = ÷ 5	Amplitudes are five times those specified for Ext Gain = 1.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TIME BASE (cont)	
Delay Time Range	
B RUNS AFTER DELAY	
SEC/DIV 50 ns and faster	
REPET ON	(0.08 x B SEC/DIV) to 1.05 ms.[a]
REPET OFF	(0.08 x B SEC/DIV) to 524 μs.[a]
SEC/DIV 50 μs to 100 ns	(0.08 x B SEC/DIV) to (65,536 x 0.08 x B SEC/DIV).[a]
SEC/DIV 100 μs and slower	(0.04 x B SEC/DIV) to (65,536 x 0.04 x B SEC/DIV).[a]
B TRIGGERABLE AFTER DELAY	
SEC/DIV 50 ns and faster	
REPET ON	16 ns to 1.05 ms.[a]
REPET OFF	8 ns to 524 μs.[a]
SEC/DIV 50 μs to 100 ns	(0.08 x B SEC/DIV) to (65,536 x 0.08 x B SEC/DIV).[a]
SEC/DIV 100 μs and slower	(0.04 x B SEC/dIV) to (65,536 x 0.04 x B SEC/DIV).[a]
Delay Time Resolution	
B RUNS AFTER DELAY	
SEC/DIV 50 μs and faster	(0.08 x B SEC/DIV).[a]
SEC/DIV 100 μs and slower	(0.04 x B SEC/DIV).[a]
B TRIGGERABLE AFTER DELAY	
SEC/DIV 50 ns and faster	
REPET ON	16 ns.[a]
REPET OFF	8 ns.[a]
SEC/DIV 50 μs to 100 ns	(0.08 x B SEC/DIV).[a]
SEC/DIV 100 μs and slower	(0.04 x B SEC/DIV).[a]
Delay Time Accuracy	±0.0015[a].

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
NONVOLATILE MEMORY	
Front-Panel Setting, Waveform Data, Sequencer, and Calibration Data Retention Time	Greater than 3 years.
Battery	3.6-volt, 1.6-Amp Hour, Lithium Thionyl Chloride; Manufacturer EAGLE PICHER, Type LTC16P/P, TEK Part Number 146-0062-00; UL Listed. (See Warning below.) **WARNING** *To avoid personal injury, observe proper procedures for handling and disposal of lithium batteries. Improper handling may cause fire, explosion, or severe burns. Don't recharge, crush, disassemble, heat the battery above 212°F (100°C), incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and national regulations.* *Typically, small quantities (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill.* *Larger quantities must be sent by surface transport to a hazardous waste disposal facility. The batteries should be individually packaged to prevent shorting and packed in a sturdy container that is clearly labeled "Lithium Batteries—DO NOT OPEN".*

Table 1-1 (cont)

Characteristics	Performance Requirements
SIGNAL OUTPUTS	
CALIBRATOR	CALIBRATOR output amplitudes at 5 MHz are at least 50% of output amplitudes at 1 ms SEC/DIV setting.[a]
Voltage (with A SEC/DIV switch set to 1 ms)	
1 MΩ Load	0.4 V ±1%.[a]
50 Ω Load	0.2 V ±1.5%.[a]
Current (short circuit load with A SEC/DIV switch set to 1 ms)	8 mA ±1.5%.[a]
Repetition Period	

A SEC/DIV Setting[a]	Calibrator Frequency[a]	Calibrator Period[a]	Div/ Cycle[a]
2 ns	5 MHz	200 ns	100
5 ns			40
10 ns			20
20 ns			10
50 ns			4
100 ns			2
200 ns			1
500 ns	1 MHz	1 μs	2
1 μs			1
2 μs			0.5
5 μs	50 kHz	20 μs	4
10 μs			2
20 μs			1
50 μs	5 kHz	200 μs	4
100 μs			2
200 μs			1
500 μs	500 Hz	2 ms	4
1 ms			2
2 ms			1
5 ms	50 Hz	20 ms	4
10 ms			2
20 ms			1
50 ms			0.4
100 ms			0.2
200 ms			0.1
500 ms			0.04
1 s			0.02
2 s			0.01
5 s			0.004

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
SIGNAL OUTPUTS (cont)	
CH 2 SIGNAL OUTPUT	
Output Voltage	20 mV per division ±10% into 1 MΩ. 10 mV per divison ±10% into 50 Ω.
Offset	±10 mV into 50 Ω, when dc balance has been performed within ±5°C of the operating temperature.
−3 dB Bandwidth	DC to greater than 50 MHz.
A TRIGGER, RECORD TRIGGER, and WORD RECOGNIZER Output	
Logic Polarity	Negative true. Trigger occurrence indicated by a HI to LO transition.[a]
Output Voltage HI	
Load of 400 μA or Less	2.5 V to 3.5 V.[a]
50 Ω Load to Ground	0.45 V or greater.[a]
Output Voltage LO	
Load of 4 mA or Less	0.5 V or less.[a]
50 Ω Load to Ground	0.15 V or less.[a]
SEQUENCE OUT, STEP COMPLETE Outputs	
Logic Polarity	Negative true. HI to LO transition indicates the event occurred.
Output Voltage HI	
Load of 400 μA or less	2.5 V to 3.5 V.[a]
50-Ω Load to Ground	0.45 V or greater.[a]
Output Voltage LO	
Load of 4 mA or less	0.5 V or less.[a]
50-Ω Load to Ground	0.15 V or less.[a]
SEQUENCE IN Input	
Logic Polarity	Negative true. HI to LO transition restarts a paused sequence.[a]
High-Level Input Current	20 μA maximum at Vin = 2.7 V.[a]
Low-Level Input Current	−0.4 mA maximum at Vin = 0.4 V.[a]
High-Level Input Voltage	2.0 V minimum.[a]
Low-level Input Voltage	0.8 V maximum.[a]
Absolute Maximum Ratings	
Vin max	+7.0 V.[a]
Vin min	−0.5 V.[a]

[a]Performance Requirements not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
DISPLAY	
Graticule	80 mm × 100 mm (8 × 10 divisions).[a]
Phosphor	P31.[a]
Nominal Accelerating Potential	16 kV.[a]
Waveform and Cursor Display, Vertical	
Resolution, Electrical	One part in 1024 (10 bit). Calibrated for 100 points per division.[a]
Gain Accuracy	Graticule indication of voltage cursor difference is within 1% of CRT cursor readout value, measured over center 6 divisions.
Centering; Vectors OFF	Within ±0.1 division.
Offset with Vectors ON	Less than 0.05 division.
Linearity	Less than 0.1 division difference between graticule indication and crt cursor readout when active volts cursor is positioned anywhere on screen and inactive cursor is at center screen.[a]
Vector Response	
NORMAL Mode	
Step Aberration	+4%, −4%, 4% p-p.
Fill	Edges of filled regions match reference lines within ±0.1 division.
ENVELOPE Mode	
Fill	Less than 1% change in p-p amplitude of a 6-division, filled ENVELOPE waveform when switching vectors ON and OFF.
Waveform and Cursor Display, Horizontal	
Resolution, Electrical	One part in 1024 (10 bit). Calibrated for 100 points per division.[a]
Gain Accuracy	Graticule indication at time cursor difference is within 1% of crt cursor readout value, measured over center 6 divisions.
Centering; Vectors OFF	Within ±0.1 division.
Offset with Vectors ON	Less than 0.05 division.
Linearity	Less than 0.1 division difference between graticule indication and crt cursor readout when active time cursor is positioned anywhere along center horizontal graticule line and inactive cursor is at center screen.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
AC POWER SOURCE	
Source Voltage	
Nominal Ranges	
115 V	90 V to 132 V.[a]
230 V	180 V to 250 V.[a]
Source Frequency	48 Hz to 440 Hz.[a]
Fuse Rating	5 A, 250 V, AGC/3AG, Fast Blow; or 4 A, 250 V, 5 × 20 mm Time-Lag (T).[a] Each fuse type requires a different fuse cap.[a]
Power Consumption	
Typical (standard instrument)	160 watts (250 VA).[a]
Maximum (fully optioned instrument)	200 watts (300 VA).[a]
Primary Grounding[c]	Type test 0.1 Ω maximum. Routine test to check grounding continuity between chassis ground and protective earth ground.[a]

[a]Performance Requirement not checked in the manual.

[c]Routine test is with ROD-L/EPA Electronic Model 100AV Hi-Pot Tester. This tests both the Primary Circuit Dielectric Withstand and Primary Grounding in one operation. Contact Tektronix Product Safety prior to using any other piece of equipment to perform these tests.

Table 1-2

Environmental Characteristics

Characteristics	Performance Requirements
STANDARD INSTRUMENT	
Environmental Requirements	This Oscilloscope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4.
Temperature	
Operating	−15°C to +55°C.
Nonoperating (storage)	−62°C to +85°C.
Altitude	
Operating	To 15,000 feet (4500 meters). Maximum operating temperature decreased 1°C for each 1000 feet (300 meters) above 5000 feet (1500 meters).
Nonoperating (storage)	To 50,000 feet (15,000 meters).
Humidity	
Operating and Storage	Stored at 95% relative humidity for five cycles (120 hours) from 30°C to 60°C, with operation performance checks at 30°C and 55°C.
Vibration	
Operating	15 minutes along each of three axes at a total displacement of 0.025 inch (0.64 mm) p-p (4 g at 55 Hz), with frequency varied from 10 Hz to 55 Hz in one-minute sweeps. Hold 10 minutes at each major resonance, or if none exist, hold 10 minutes at 55 Hz (75 minutes total test time).
Shock	
Operating and Nonoperating	50-g, half-sine, 11-ms duration, three shocks on each face, for a total of 18 shocks.
Transit Drop (not in shipping package)	12-inch (300-mm) drop on each corner and each face (exceeds MIL-T-28800C, paragraphs 3.9.5.2 and 4.5.5.4.2).
Bench Handling	
Cabinet On and Cabinet Off	MIL-STD-810C, Method 516.2, Procedure V (MIL-T-28800C, Paragraph 4.5.5.4.3).
Topple (cabinet installed)	
Operating	Set on rear feet and allow to topple over onto each of four adjacent faces (Tektronix Standard 062-2858-00).
Packaged Transportation	
Drop	Meets the limits of the National Safe Transit Assn., test procedure 1A-B-2; 10 drops of 36 inches (914 mm) (Tektronix Standard 062-2858-00).
Vibration	Meets the limits of the National Safe Transit Assn., test procedure 1A-B-1; excursion of 1 inch (25.4 mm) p-p at 4.63 Hz (1.1 g) for 30 minutes (Tektronix Standard 062-2858-00).

Table 1-2 (cont)

Characteristics	Performance Requirements
STANDARD INSTRUMENT (cont)	
Environmental Requirements (cont)	
EMI (electromagnetic interference)	Meets MIL-T-28800C; MIL-STD-461B, part 4 (CE-03 and CS-02), part 5 (CS-06 and RS-02), and part 7 (CS-01, RE-02, and RS-03—limited to 1 GHz); VDE 0871, Category B; Part 15 of FCC Rules and Regulations, Subpart J, Class A; and Tektronix Standard 062-2866-00.
Electrostatic Discharge Susceptibility	Meets Tektronix Standard 062-2862-00. The instrument will not change control states with discharges of less than 10 kV.
X-Ray Radiation	Meets requirements of Tektronix Standard 062-1860-00.
RACKMOUNTED INSTRUMENT	
Environmental Requirements	Listed characteristics for vibration and shock indicate those environments in which the rackmounted instrument meets or exceeds the requirements of MIL-T-28800C with respect to Type III, Class 5, Style D equipment with the rackmounting rear-support kit installed. Refer to the Standard Instrument Environmental Specification for the remaining performance requirements. Instruments will be capable of meeting or exceeding the requirements of Tektronix Standard 062-2853-00, class 5.
Temperature (operating)	−15°C to +55°C, ambient temperature measured at the instrument's air inlet. Fan exhaust temperature should not exceed +65°C.
Vibration	15 minutes along each of three major axes at a total displacement of 0.015 inch (0.38 mm) p-p (2.3 g at 55 Hz), with frequency varied from 10 Hz to 55 Hz to 10 Hz in one-minute sweeps. Hold 10 minutes at each major resonance, or if no major resonance is present, hold 10 minutes at 55 Hz (75 minutes total test time).
Shock (operating and nonoperating)	30-g, half-sine, 11-ms duration, three shocks per axis in each direction, for a total of 18 shocks.

Table 1-3

Mechanical Characteristics

Characteristics	Description
STANDARD INSTRUMENT	
Weight	
With Front Cover, Accessories, and Accessories Pouch	≃12.8 kg (28.1 lbs).
Without Front Cover, Accessories, and Accessories Pouch	≃10.9 kg (23.9 lbs).
Domestic Shipping Weight	≃16.4 kg (36 lbs).
Overall Dimensions	See Figure 1-1 for a dimensional drawing.
Height	
With Feet and Accessories Pouch	190 mm (7.48 in).
Without Accessories Pouch	160 mm (6.3 in).
Width (with handle)	330 mm (13.0 in).
Depth	
With Front Cover	479 mm (18.86 in).
With Handle Extended	550 mm (21.65 in).
Cooling	Forced air circulation; no air filter.
Finish	Tektronix Blue vinyl-clad material on aluminum cabinet.
Construction	Aluminum-alloy/plastic-composite chassis (spot-molded). Plastic-laminate front panel. Glass-laminate circuit boards.
RACKMOUNTING	
Rackmounting Conversion Kit	
Weight	4.0 kg (8.8 lbs).
Domestic Shipping Weight	6.3 kg (13.8 lbs).
Height	178 mm (7 in).
Width	483 mm (19 in).
Depth	419 mm (16.5 in).
Rear Support Kit	
Weight	0.68 kg (1.5 lbs).
OPTION 1R	
Rackmounted Instrument (Option 1R)	
Weight	≃15.8 kg (34.9 lbs).
Domestic Shipping Weight	≃18.1 kg (39.9 lbs).
Height	178 mm (7 in).
Width	483 mm (19 in).
Depth	419 mm (16.5 in).

Table 1-4

Option 05 (TV Trigger) Electrical Characteristics

Characteristics	Performance Requirements
VERTICAL—CHANNEL 1 AND CHANNEL 2	
Frequency Response	
Full Bandwidth	
50 kHz to 5 MHz	Within ±1%.
Greater than 5 MHz to 10 MHz	Within +1%, −2%.
Greater than 10 MHz to 30 MHz	Within +2%, −3%. For VOLTS/DIV switch settings between 5 mV and 0.2 V per division with VARIABLE VOLTS/DIV set to CAL. Five-division, 50 kHz reference signals from a 50 Ω system. With external 50 Ω termination on a 1 MΩ input.
20 MHz Bandwidth Limit	
50 kHz to 5 MHz	Within +1%, −4%.
Square Wave Flatness	
Field Rate	
5 mV/div to 20 mV/div	±1%, 1% p-p at 60 Hz with input signal of 0.1 V.
50 mV/div	±1%, 1% p-p at 60 Hz with input signal of 1.0 V. With fast-rise step (rise time 1 ns or less), 1 MΩ dc input coupling, an external 50 Ω termination, and VARIABLE VOLTS/DIV set to CAL. Exclude the first 20 ns following the step transition and exclude the first 30 ns when 20 MHz BW LIMIT is set.
Line Rate	
5 mV/div to 20 mV/div	±1%, 1% p-p at 15 kHz with input signal of 0.1 V.
50 mV/div	±1%, 1% p-p at 15 kHz with input signal of 1.0 V.
TV (Back-Porch) Clamp (CH 2 Only)	
60 Hz Attenuation	18 dB or greater. For VOLTS/DIV switch settings between 5 mV and 0.2 V with VARIABLE VOLTS/DIV set to CAL. Six-division reference signal.
Back-Porch Reference	Within ±1.0 division of ground reference.

Table 1-4 (cont)

Characteristics	Performance Requirements
TRIGGERING	
Sync Separation	Stable video rejection and sync separation from sync-positive or sync-negative composite video, 525 to 1280 lines, 50 Hz or 60 Hz, interlaced or noninterlaced systems.
Trigger Modes	
A Horizontal Mode	All lines: Field 1, selected line (1 to n), Field 2, selected line (1 to n), Alt fields, selected line (1 to n). n is equal to or less than the number of lines in the frame and less than or equal to 1280.
B Horizontal Mode	Delayed by time.
Minimum Input Signal Amplitude for Stable Triggering[a,b]	
Channel 1 and Channel 2	
Composite Video	2 divisions.
Composite Sync	0.6 divisions. Peak signal amplitude within 18 divisions of input ground reference.
EXT TRIG 1 or EXT TRIG 2	
EXT GAIN = 1	
Composite Video	60 mV.
Composite Sync	30 mV. Peak signal amplitude within ±0.9 V from input ground reference.
EXT GAIN = ÷5	
Composite Video	300 mV.
Composite Sync	150 mV Peak signal amplitude within ±4.9 V from input ground reference.

[a]**Performance Requirement not checked in manual.**

[b]**A stable trigger is one that results in a uniform, regular display triggered on the selected slope (±). A stably-triggered display should NOT have the trigger point switch between opposite slopes on the waveform, nor should it "roll" across the screen, as successive acquisitions occur. At TIME/DIV settings of 2 ms/DIV and faster, the TRIG'D LED is constantly lit if the display is stably triggered (the LED can flash for SEC/DIV settings of 10 ms/DIV and slower).**

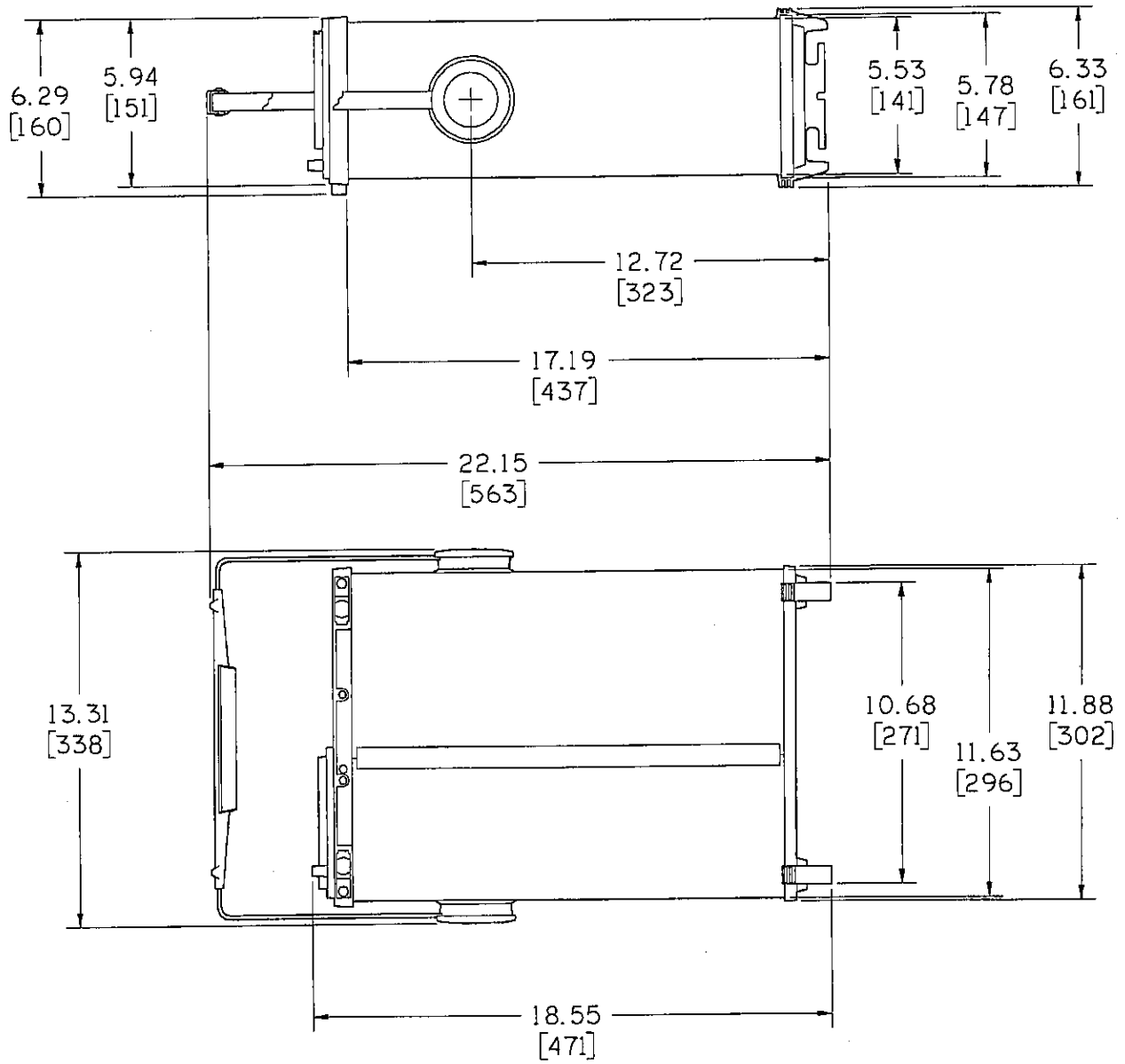


Figure 1-1. Dimensional drawing.

PREPARATION FOR USE

SAFETY

This section tells how to prepare for and to proceed with the initial start-up of the TEKTRONIX 2440 Digital Oscilloscope.

Refer to the Operators and Servicing Safety Summaries at the front of this manual for power source, grounding, and other safety considerations pertaining to the use of the instrument. Before connecting the oscilloscope to a power source, read both this section and the Safety Summaries.

CAUTION

This instrument may be damaged if operated with the LINE VOLTAGE SELECTOR switch set for the wrong applied ac input-source voltage or if the wrong line fuse is installed.

LINE VOLTAGE SELECTION

The scope operates from either a 115 V or 230 V nominal ac power-input source having a line frequency ranging from 48 Hz to 440 Hz. Before connecting the power cord to a power-input source, verify that the LINE VOLTAGE SELECTOR switch, located on the rear panel (see Figure 2-1), is set for the correct nominal ac input-source voltage. To convert the instrument for operation from one line-voltage range to the other, move the LINE VOLTAGE SELECTOR switch to the correct nominal ac source-voltage setting (see Table 2-1). The detachable power cord may have to be changed to match the particular power-source outlet.

LINE FUSE

To verify the proper value of the instrument's power-input fuse, perform the following procedure:

1. Press in the fuse-holder cap and release it with a slight counterclockwise rotation.

2. Pull the cap (with the attached fuse inside) out of the fuse holder.

3. Verify proper fuse value (see Table 2-1).

4. Install the proper fuse and reinstall the fuse-holder cap.

NOTE

A 4 A, 250 V, 5 × 20 mm Time-lag (T) fuse may be substituted for the factory-installed fuse. However, the two types of fuses are NOT directly interchangeable; each requires a different type of fuse cap.

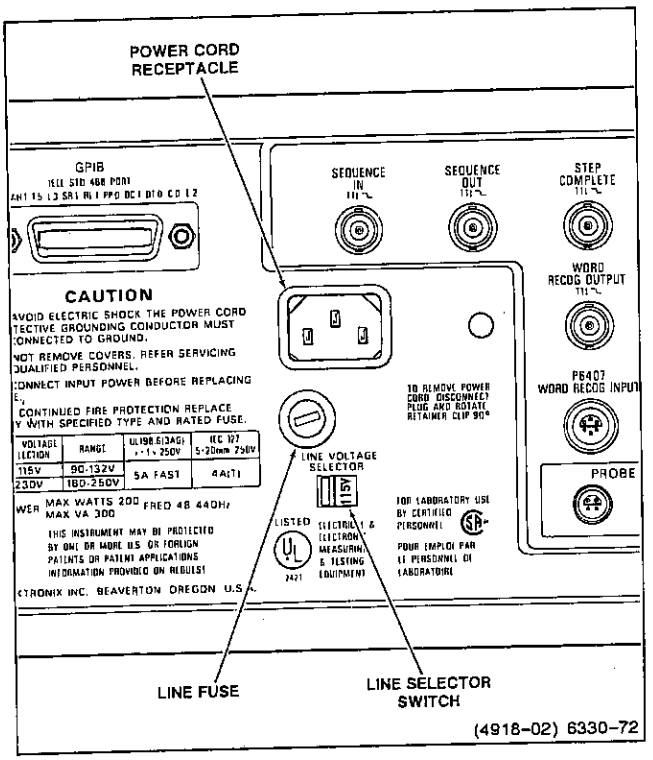
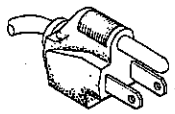
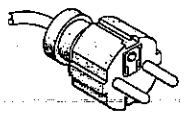
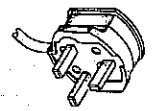
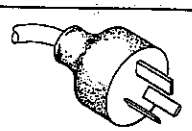
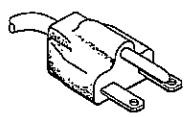
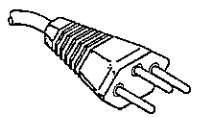


Figure 2-1. LINE VOLTAGE SELECTOR, line fuse, and power cord receptacle.

Table 2-1

Voltage, Fuse, and Power-Cord Data

Plug Configuration	Category	Power Cord And Plug Type	Line Voltage Selector Setting	Voltage Range (AC)	Factory Installed Instrument Fuse	Fuse Holder Cap	Reference Standards[b]
	U.S. Domestic Standard	U.S. 120V 15A	115V	90V to 132V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.11 NEMA 5-15-P UL 198.6
	Option A1	EURO 240V 10-16A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	CEE(7), II, IV, VII IEC 83 IEC 127
	Option A2	UK[a] 240V 6A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	BS 1363 IEC 83 IEC 127
	Option A3	Australian 240V 10A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	AS C112 IEC 127
	Option A4	North American 240V 15A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.20 NEMA 6-15-P IEC 83 UL 198.6
	Option A5	Switzerland 220V 6A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	SEV IEC 127

[a] A 6A, Type C fuse is also installed inside the plug of the Option A2 power cord.

[b] Reference Standards Abbreviations:

ANSI—American National Standards Institute
AS—Standards Association of Australia
BS—British Standards Institution
CEE—International Commission on Rules for the Approval of Electrical Equipment
IEC—International Electrotechnical Commission
NEMA—National Electrical Manufacturer's Association
SEV—Schweizevischer Elektrotechischer Verein
UL—Underwriters Laboratories Inc.

4918-03

POWER CORD

This instrument has a detachable three-wire power cord with a three-contact plug for connection to both the power source and protective ground. The power cord is secured to the rear panel by a cord-set securing clamp. The protective ground contact on the plug connects (through the power cord protective grounding conductor) to the accessible metal parts of the instrument. For protection against electrical shock, insert this plug into a power-source outlet that has a properly grounded protective-ground contact.

Instruments are shipped with the required power cord as ordered by the customer. Information on the available power cords is presented in Table 2-1, and part numbers are listed in "Options and Accessories" (Section 7). Contact your Tektronix representative or local Tektronix Field Office for additional power-cord information.

INSTRUMENT COOLING

To prevent instrument damage from overheated components, adequate internal airflow must be maintained. Before turning on the power, first verify that air-intake holes on the bottom and side of the cabinet and the fan exhaust holes are free of any obstruction to airflow. The scope has a thermal cutout that will activate if overheating occurs. The scope shuts down immediately with no attempt to save waveforms or front-panel conditions if a cutout happens. Power will be disabled to the scope until the thermal cutout cools down, at which time the power-on sequence is redone. The resulting loss of the last front-panel and waveform data will cause the power-on self test to fail and is indicated to the user by a failed CKSUM-NVRAM test (number 6000 in the main EXTENDED DIAGNOSTICS menu). The cause of the overheating must be corrected before attempting prolonged operation of the scope. Pressing the MENU OFF/EXTENDED FUNCTIONS button restores the scope to the normal operating mode.

START-UP

This instrument automatically performs power-up tests each time the instrument is turned on. These tests provide the highest possible confidence level that the instrument is fully functional. If no faults are encountered, the instrument will enter the Scope mode in the either ACQUIRE or SAVE Storage mode, depending on the mode in effect when it was powered off.

If tests are failed, the scope displays the Extended Diagnostics menu. If the failure is in the range of 1000-5300 and the message "HARDWARE PROBLEM—SEE SERVICE MANUAL" is displayed with the menu, see "Diagnostics" in Section 6 for more information. If the failure is in 1000-5300 range, but "RUN SELF CAL WHEN WARMED UP" is displayed, the SELF CAL procedure should be executed from the EXTENDED FUNCTIONS menu (wait for the NOT WARMED UP message to disappear from the SELF CAL menu). If failures persist after the SELF CAL is run (the "HARDWARE PROBLEM—SEE SERVICE MANUAL" message will be displayed), see "Diagnostics" in Section 6 for more information.

Failure of a test in the range of 7000 to 9300 may not indicate a fatal scope fault. Several conditions can occur that will cause a non-fatal failure of the tests. The scope will display "RUN SELF CAL WHEN WARMED UP" to indicate a SELF CAL should be performed. If SELF CAL does not clear the failure ("HARDWARE PROBLEM—SEE SERVICE MANUAL" is displayed), the scope may still be usable for your immediate measurement purposes. For example, if the problem area is in CH 2, CH 1 may still be used with full confidence of making accurate measurements. Press the MENU OFF/EXTENDED FUNCTIONS button to exit EXTENDED DIAGNOSTICS and enter Scope mode.

NOTE

The SELF CAL procedure is detailed in Section 5 of this manual. Refer to Section 6 of this manual for information on the power-up tests and the procedures to follow in the event of a failed power-up test.

A fatal fault in the operating system will cause the scope to abort. No displays are possible, and the user is notified of an abort situation only by the flashing of the Trigger LED indicators (if that is possible). Cycling the power off then back on may clear the problem, but a failure of this magnitude usually requires the scope to be referred to a qualified service person for checkout and repairs. Persistent or reoccurring failures of the power-on or self-diagnostic tests should be brought to the attention of a qualified service person at the first opportunity. Consult your service department, your local Tektronix Service Center, or nearest Tektronix representative if further assistance is needed.

POWER-DOWN

NOTE

POWER INTERRUPTION TO THE INSTRUMENT WHEN THE SELF-CALIBRATION ROUTINE IS EXECUTING INVALIDATES THE INSTRUMENT CALIBRATION CONSTANTS. Upon such an interruption, the instrument sets an internal flag denoting that SELF CAL was running at shutdown. When power is reestablished, the scope will display "RUN SELF CAL WHEN WARMED UP". When the "NOT WARMED UP" message disappears from the SELF CAL menu, the user MUST perform a SELF CAL to escape the EXT DIAG menu (the ↑ menu button MUST be used to access the SELF CAL menu—see Section 6 for more information). If failures persist after the SELF CAL is performed, refer the instrument to qualified service personnel.

For a normal power-off from the scope mode, an orderly power-down sequence retains the SAVE and SAVEREF waveforms, the current front-panel control settings, and any stored front-panel settings. If a power-off or transient power fluctuation occurs during SELF CAL, or EXTENDED CALIBRATION, or the instrument shuts-down at any time due to overheating, the normal power-down sequence is not executed. The result is loss of stored calibration constants or last front-panel control settings (or both) and a failure of the next power-on self-test (6000-6400 range). If front panel, sequencer, or stored waveform information was lost, the error will clear itself on the next power-down/power-up cycle. If calibration constants were lost the instrument will display information indicating if calibration is needed.

If power is momentarily interrupted, starting the power-off sequence, but is reestablished before the sequence completes, the scope will redo the power-on procedure. If the scope is in the middle of a waveform acquisition when power interruption occurs, the waveform data will not be saved, and the invalid waveform data display will be seen when power-on has completed. Press ACQUIRE to restart the acquisition and obtain valid waveform data.

REPACKAGING FOR SHIPMENT

It is recommended that the original carton and packing material be saved in the event it is necessary for the instrument to be reshipped using a commercial transport carrier. If the original materials are unfit or not available, then repackage the instrument using the following procedure.

1. Use a corrugated cardboard shipping carton having a test strength of at least 275 pounds and with an inside dimension at least six inches greater than the instrument dimensions.

2. If the instrument is being shipped to a Tektronix Service Center, enclose the following information: the owner's address, name and phone number of a contact person, type and serial number of the instrument, reason for returning, and a complete description of the service required.

3. Completely wrap the instrument with polyethylene sheeting or equivalent to protect the outside finish and prevent entry of harmful substances into the instrument.

4. Cushion instrument on all sides using three inches of padding material or urethane foam, tightly packed between the carton and the instrument.

5. Seal the shipping carton with an industrial stapler or strapping tape.

6. Mark the address of the Tektronix Service Center and also your own return address on the shipping carton in two prominent locations.

POWER-DOWN

NOTE

POWER INTERRUPTION TO THE INSTRUMENT WHEN THE SELF-CALIBRATION ROUTINE IS EXECUTING INVALIDATES THE INSTRUMENT CALIBRATION CONSTANTS. Upon such an interruption, the instrument sets an internal flag denoting that SELF CAL was running at shutdown. When power is reestablished, the scope will display "RUN SELF CAL WHEN WARMED UP". When the "NOT WARMED UP" message disappears from the SELF CAL menu, the user MUST perform a SELF CAL to escape the EXT DIAG menu (the ↑ menu button MUST be used to access the SELF CAL menu—see Section 6 for more information). If failures persist after the SELF CAL is performed, refer the instrument to qualified service personnel.

For a normal power-off from the scope mode, an orderly power-down sequence retains the SAVE and SAVEREF waveforms, the current front-panel control settings, and any stored front-panel settings. If a power-off or transient power fluctuation occurs during SELF CAL, or EXTENDED CALIBRATION, or the instrument shuts-down at any time due to overheating, the normal power-down sequence is not executed. The result is loss of stored calibration constants or last front-panel control settings (or both) and a failure of the next power-on self-test (6000-6400 range). If front panel, sequencer, or stored waveform information was lost, the error will clear itself on the next power-down/power-up cycle. If calibration constants were lost the instrument will display information indicating if calibration is needed.

If power is momentarily interrupted, starting the power-off sequence, but is reestablished before the sequence completes, the scope will redo the power-on procedure. If the scope is in the middle of a waveform acquisition when power interruption occurs, the waveform data will not be saved, and the invalid waveform data display will be seen when power-on has completed. Press ACQUIRE to restart the acquisition and obtain valid waveform data.

REPACKAGING FOR SHIPMENT

It is recommended that the original carton and packing material be saved in the event it is necessary for the instrument to be reshipped using a commercial transport carrier. If the original materials are unfit or not available, then repackage the instrument using the following procedure.

1. Use a corrugated cardboard shipping carton having a test strength of at least 275 pounds and with an inside dimension at least six inches greater than the instrument dimensions.

2. If the instrument is being shipped to a Tektronix Service Center, enclose the following information: the owner's address, name and phone number of a contact person, type and serial number of the instrument, reason for returning, and a complete description of the service required.

3. Completely wrap the instrument with polyethylene sheeting or equivalent to protect the outside finish and prevent entry of harmful substances into the instrument.

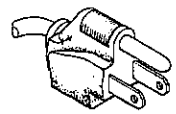
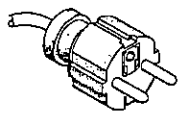
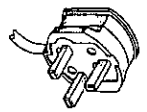
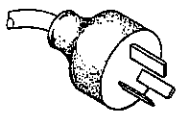
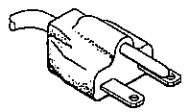
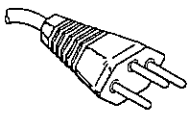
4. Cushion instrument on all sides using three inches of padding material or urethane foam, tightly packed between the carton and the instrument.

5. Seal the shipping carton with an industrial stapler or strapping tape.

6. Mark the address of the Tektronix Service Center and also your own return address on the shipping carton in two prominent locations.

Table 2-1

Voltage, Fuse, and Power-Cord Data

Plug Configuration	Category	Power Cord And Plug Type	Line Voltage Selector Setting	Voltage Range (AC)	Factory Installed Instrument Fuse	Fuse Holder Cap	Reference Standards[b]
	U.S. Domestic Standard	U.S. 120V 15A	115V	90V to 132V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.11 NEMA 5-15-P UL 198.6
	Option A1	EURO 240V 10-16A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	CEE(7), II, IV, VII IEC 83 IEC 127
	Option A2	UK[a] 240V 6A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	BS 1363 IEC 83 IEC 127
	Option A3	Australian 240V 10A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	AS C112 IEC 127
	Option A4	North American 240V 15A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.20 NEMA 6-15-P IEC 83 UL 198.6
	Option A5	Switzerland 220V 6A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	SEV IEC 127

[a] A 6A, Type C fuse is also installed inside the plug of the Option A2 power cord.

[b] Reference Standards Abbreviations:

ANSI—American National Standards Institute
AS—Standards Association of Australia
BS—British Standards Institution
CEE—International Commission on Rules for the Approval of Electrical Equipment
IEC—International Electrotechnical Commission
NEMA—National Electrical Manufacturer's Association
SEV—Schweizevischer Elektrotechischer Verein
UL—Underwriters Laboratories Inc.

4918-03

Table 1-4 (cont)

Characteristics	Performance Requirements
TRIGGERING	
Sync Separation	Stable video rejection and sync separation from sync-positive or sync-negative composite video, 525 to 1280 lines, 50 Hz or 60 Hz, interlaced or noninterlaced systems.
Trigger Modes	
A Horizontal Mode	All lines: Field 1, selected line (1 to n), Field 2, selected line (1 to n), Alt fields, selected line (1 to n). n is equal to or less than the number of lines in the frame and less than or equal to 1280.
B Horizontal Mode	Delayed by time.
Minimum Input Signal Amplitude for Stable Triggering[a,b]	
Channel 1 and Channel 2	
Composite Video	2 divisions.
Composite Sync	0.6 divisions. Peak signal amplitude within 18 divisions of input ground reference.
EXT TRIG 1 or EXT TRIG 2	
EXT GAIN = 1	
Composite Video	60 mV.
Composite Sync	30 mV. Peak signal amplitude within ±0.9 V from input ground reference.
EXT GAIN = ÷5	
Composite Video	300 mV.
Composite Sync	150 mV Peak signal amplitude within ±4.9 V from input ground reference.

[a]Performance Requirement not checked in manual.

[b]A stable trigger is one that results in a uniform, regular display triggered on the selected slope (±). A stably-triggered display should NOT have the trigger point switch between opposite slopes on the waveform, nor should it "roll" across the screen, as successive acquisitions occur. At TIME/DIV settings of 2 ms/DIV and faster, the TRIG'D LED is constantly lit if the display is stably triggered (the LED can flash for SEC/DIV settings of 10 ms/DIV and slower).

Table 1-3

Mechanical Characteristics

Characteristics	Description
STANDARD INSTRUMENT	
Weight	
With Front Cover, Accessories, and Accessories Pouch	≃12.8 kg (28.1 lbs).
Without Front Cover, Accessories, and Accessories Pouch	≃10.9 kg (23.9 lbs).
Domestic Shipping Weight	≃16.4 kg (36 lbs).
Overall Dimensions	See Figure 1-1 for a dimensional drawing.
Height	
With Feet and Accessories Pouch	190 mm (7.48 in).
Without Accessories Pouch	160 mm (6.3 in).
Width (with handle)	330 mm (13.0 in).
Depth	
With Front Cover	479 mm (18.86 in).
With Handle Extended	550 mm (21.65 in).
Cooling	Forced air circulation; no air filter.
Finish	Tektronix Blue vinyl-clad material on aluminum cabinet.
Construction	Aluminum-alloy/plastic-composite chassis (spot-molded). Plastic-laminate front panel. Glass-laminate circuit boards.
RACKMOUNTING	
Rackmounting Conversion Kit	
Weight	4.0 kg (8.8 lbs).
Domestic Shipping Weight	6.3 kg (13.8 lbs).
Height	178 mm (7 in).
Width	483 mm (19 in).
Depth	419 mm (16.5 in).
Rear Support Kit	
Weight	0.68 kg (1.5 lbs).
OPTION 1R	
Rackmounted Instrument (Option 1R)	
Weight	≃15.8 kg (34.9 lbs).
Domestic Shipping Weight	≃18.1 kg (39.9 lbs).
Height	178 mm (7 in).
Width	483 mm (19 in).
Depth	419 mm (16.5 in).

Table 1-2

Environmental Characteristics

Characteristics	Performance Requirements
STANDARD INSTRUMENT	
Environmental Requirements	This Oscilloscope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4.
Temperature	
Operating	−15°C to +55°C.
Nonoperating (storage)	−62°C to +85°C.
Altitude	
Operating	To 15,000 feet (4500 meters). Maximum operating temperature decreased 1°C for each 1000 feet (300 meters) above 5000 feet (1500 meters).
Nonoperating (storage)	To 50,000 feet (15,000 meters).
Humidity	
Operating and Storage	Stored at 95% relative humidity for five cycles (120 hours) from 30°C to 60°C, with operation performance checks at 30°C and 55°C.
Vibration	
Operating	15 minutes along each of three axes at a total displacement of 0.025 inch (0.64 mm) p-p (4 g at 55 Hz), with frequency varied from 10 Hz to 55 Hz in one-minute sweeps. Hold 10 minutes at each major resonance, or if none exist, hold 10 minutes at 55 Hz (75 minutes total test time).
Shock	
Operating and Nonoperating	50-g, half-sine, 11-ms duration, three shocks on each face, for a total of 18 shocks.
Transit Drop (not in shipping package)	12-inch (300-mm) drop on each corner and each face (exceeds MIL-T-28800C, paragraphs 3.9.5.2 and 4.5.5.4.2).
Bench Handling	
Cabinet On and Cabinet Off	MIL-STD-810C, Method 516.2, Procedure V (MIL-T-28800C, Paragraph 4.5.5.4.3).
Topple (cabinet installed)	
Operating	Set on rear feet and allow to topple over onto each of four adjacent faces (Tektronix Standard 062-2858-00).
Packaged Transportation	
Drop	Meets the limits of the National Safe Transit Assn., test procedure 1A-B-2; 10 drops of 36 inches (914 mm) (Tektronix Standard 062-2858-00).
Vibration	Meets the limits of the National Safe Transit Assn., test procedure 1A-B-1; excursion of 1 inch (25.4 mm) p-p at 4.63 Hz (1.1 g) for 30 minutes (Tektronix Standard 062-2858-00).

Table 1-1 (cont)

Characteristics	Performance Requirements
DISPLAY	
Graticule	80 mm × 100 mm (8 × 10 divisions).[a]
Phosphor	P31.[a]
Nominal Accelerating Potential	16 kV.[a]
Waveform and Cursor Display, Vertical	
Resolution, Electrical	One part in 1024 (10 bit). Calibrated for 100 points per division.[a]
Gain Accuracy	Graticule indication of voltage cursor difference is within 1% of CRT cursor readout value, measured over center 6 divisions.
Centering; Vectors OFF	Within ±0.1 division.
Offset with Vectors ON	Less than 0.05 division.
Linearity	Less than 0.1 division difference between graticule indication and crt cursor readout when active volts cursor is positioned anywhere on screen and inactive cursor is at center screen.[a]
Vector Response	
NORMAL Mode	
Step Aberration	+4%, −4%, 4% p-p.
Fill	Edges of filled regions match reference lines within ±0.1 division.
ENVELOPE Mode	
Fill	Less than 1% change in p-p amplitude of a 6-division, filled ENVELOPE waveform when switching vectors ON and OFF.
Waveform and Cursor Display, Horizontal	
Resolution, Electrical	One part in 1024 (10 bit). Calibrated for 100 points per division.[a]
Gain Accuracy	Graticule indication at time cursor difference is within 1% of crt cursor readout value, measured over center 6 divisions.
Centering; Vectors OFF	Within ±0.1 division.
Offset with Vectors ON	Less than 0.05 division.
Linearity	Less than 0.1 division difference between graticule indication and crt cursor readout when active time cursor is positioned anywhere along center horizontal graticule line and inactive cursor is at center screen.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
SIGNAL OUTPUTS	
CALIBRATOR	CALIBRATOR output amplitudes at 5 MHz are at least 50% of output amplitudes at 1 ms SEC/DIV setting.[a]
Voltage (with A SEC/DIV switch set to 1 ms)	
1 MΩ Load	0.4 V ±1%.[a]
50 Ω Load	0.2 V ±1.5%.[a]
Current (short circuit load with A SEC/DIV switch set to 1 ms)	8 mA ±1.5%.[a]

Repetition Period

A SEC/DIV Setting[a]	Calibrator Frequency[a]	Calibrator Period[a]	Div/ Cycle[a]
2 ns	5 MHz	200 ns	100
5 ns			40
10 ns			20
20 ns			10
50 ns			4
100 ns			2
200 ns			1
500 ns	1 MHz	1 μs	2
1 μs			1
2 μs			0.5
5 μs	50 kHz	20 μs	4
10 μs			2
20 μs			1
50 μs	5 kHz	200 μs	4
100 μs			2
200 μs			1
500 μs	500 Hz	2 ms	4
1 ms			2
2 ms			1
5 ms	50 Hz	20 ms	4
10 ms			2
20 ms			1
50 ms			0.4
100 ms			0.2
200 ms			0.1
500 ms			0.04
1 s			0.02
2 s			0.01
5 s			0.004

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TIME BASE (cont)	
Delay Time Range	
B RUNS AFTER DELAY	
SEC/DIV 50 ns and faster	
REPET ON	(0.08 x B SEC/DIV) to 1.05 ms.[a]
REPET OFF	(0.08 x B SEC/DIV) to 524 μs.[a]
SEC/DIV 50 μs to 100 ns	(0.08 x B SEC/DIV) to (65,536 x 0.08 x B SEC/DIV).[a]
SEC/DIV 100 μs and slower	(0.04 x B SEC/DIV) to (65,536 x 0.04 x B SEC/DIV).[a]
B TRIGGERABLE AFTER DELAY	
SEC/DIV 50 ns and faster	
REPET ON	16 ns to 1.05 ms.[a]
REPET OFF	8 ns to 524 μs.[a]
SEC/DIV 50 μs to 100 ns	(0.08 x B SEC/DIV) to (65,536 x 0.08 x B SEC/DIV).[a]
SEC/DIV 100 μs and slower	(0.04 x B SEC/dIV) to (65,536 x 0.04 x B SEC/DIV).[a]
Delay Time Resolution	
B RUNS AFTER DELAY	
SEC/DIV 50 μs and faster	(0.08 x B SEC/DIV).[a]
SEC/DIV 100 μs and slower	(0.04 x B SEC/DIV).[a]
B TRIGGERABLE AFTER DELAY	
SEC/DIV 50 ns and faster	
REPET ON	16 ns.[a]
REPET OFF	8 ns.[a]
SEC/DIV 50 μs to 100 ns	(0.08 x B SEC/DIV).[a]
SEC/DIV 100 μs and slower	(0.04 x B SEC/DIV).[a]
Delay Time Accuracy	±0.0015[a].

[a]**Performance Requirement not checked in the manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements		
TRIGGERING—A and B (cont)			
Variable A Trigger Holdoff	**A SEC/DIV[a]**	**MIN HO[a]**	**MAX HO[a]**
	500 ns	5-10 μs	
	1 μs 2 μs 5 μs	10-20 μs 20-40 μs 50-100 μs	100-150 μs
	10 μs 20 μs 50 μs	0.1-0.2 ms 0.2-0.4 ms 0.5-1.0 ms	1-1.5 ms
	100 μs 200 μs 500 μs	1-2 ms 2-4 ms 5-10 ms	10-15 ms
	1 ms 2 ms 5 ms	10-20 ms 20-40 ms 50-100 ms	90-150 ms
	10 ms 20 ms 50 ms	0.1-0.2 s 0.2-0.4 s 0.5-1.0 s	0.9-1.5 s
	100 ms 200 ms	1-2 s 2-4 s	9-15 s
	500 ms 1 s 2 s 5 s	5-10 s	
SLOPE Selection	Conforms to trigger-source and ac-power-source waveforms.		
Trigger Position Jitter (P-P)	Checked in NORMAL ACQUIRE mode with a 5-division step having less than or equal to 1 ns rise time.		
A Mode, B Mode (TRIG AFTER)			
SEC/DIV 100 ns and slower	0.04 x SEC/DIV setting[a,b]		
SEC/DIV 50 ns and faster	(0.04 x SEC/DIV setting) + 200 ps[a,b]		
B Mode (RUNS AFTER)			
SEC/DIV 50 ns and faster	(0.04 x B SEC/DIV + 200 ps[a]		
SEC/DIV 50 μs to 100 ns	0.04 x B SEC/DIV[a]		
SEC/DIV 100 μs and slower	0.08 x B SEC/DIV[a]		

[a]Performance Requirements not checked in the manual.

[b]Use B SEC/DIV setting if mode is B; otherwise, use A SEC/DIV setting.

Table 1-1 (cont)

Characteristics	Performance Requirements
TRIGGERING—A and B (cont)	
Maximum P-P Signal Rejected by NOISE REJ Coupling Signals within the Vertical Bandwidth	
Channel 1 or Channel 2 Source	0.4 division or greater for VOLTS/DIV settings of 10 mV and higher. Maximum noise rejected is reduced at 2 mV per division and 5 mV per division.
EXT TRIG 1 or EXT TRIG 2 Source	20 mV or greater when Ext Trig Gain = 1. 100 mV or greater when Ext Trig Gain = ÷5.
EXT TRIG 1 and EXT TRIG 2 Inputs	
Resistance	1 MΩ ±1%.[a]
Capacitance	15 pF ±3 pF.[a]
Maximum Input Voltage ⚠	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
LEVEL Control Range	
Channel 1 or Channel 2 Source	±18 divisions × VOLTS/DIV setting.[a]
EXT TRIG 1 or EXT TRIG 2 Source	
EXT GAIN = 1	±0.9 volt.[a]
EXT GAIN = ÷5	±4.5 volts.[a]
LEVEL Readout Accuracy (for triggering signals with transition times greater than 20 ns)	
Channel 1 or Channel 2 Source	
DC Coupled	
+15°C to +35°C	Within ± [3% of setting + 3% of p-p signal + (0.2 division × VOLTS/DIV setting) + 0.5 mV + (0.5 mV × probe attenuation factor)].
−15°C to +55°C (excluding +15°C to +35°C)	Add (1.5 mV × probe attenuation) to +15°C to +35°C specification.[a]
NOISE REJ Coupled	Add ± (0.6 division × VOLTS/DIV setting) to DC Coupled specifications. Checked at 50 mV per division.

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
ACQUISITION SYSTEM—CHANNEL 1 AND CHANNEL 2 (cont)	
Maximum Input Voltages ⚠	
Input Coupling Set to DC, AC, or GND	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
Common-Mode Rejection Ratio (CMRR); ADD Mode with Either Channel Inverted	At least 10:1 at 50 MHz for common-mode signals of 10 divisions or less with VARIABLE VOLTS/DIV adjusted for best CMRR at 50 kHz.
POSITION	
Range	± (9.3 to 10.4) div., at 50 mV per division with INVERT off, when Self Cal has been done within ±5°C of the operating temperature.
Gain Match between NORMAL and SAVE	±3 DLs for positions within ±5 divisions from center.
Low-Frequency Linearity	
Normal or Average Mode	3 DLs or less compression or expansion of a two-division, center-screen signal when positioned anywhere within the acquisition window.
20-MHz Bandwidth Limiter	
−3 dB Bandwidth	13 MHz to 24 MHz.
100-MHz Bandwidth Limiter	
−3 dB Bandwidth	80 MHz to 120 MHz.
Rise Time	2.9 ns to 4.4 ns.[a]
	With a five-division, fast-rise step (rise time of 300 ps or less) using 50-Ω dc input coupling and VOLTS/DIV setting of 10 mV.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
ACQUISITION SYSTEM—CHANNEL 1 AND CHANNEL 2 (cont)	
Bandwidth	Bandwidth is measured with a leveled, low distortion, 50-Ω source, sine-wave generator, terminated in 50 Ω. The reference signal is set to 6 divisions or to the maximum leveled amplitude obtainable if the Volt/Div setting is too high to yield 6 div's on screen. Bandwidth with probe is checked using a probe-tip-to-GR termination adaptor (017-0520-00). Bandwidth with external termination is checked using a BNC 50-Ω feed-through terminator (011-0049-01).
−3 dB Bandwidth	
Normal or Average Modes. Envelope Mode at SEC/DIV settings of 0.2 μs or faster.	Using standard accessory probe or internal termination (not checked with probe in manual).
−15°C to +30°C	Dc to 300 MHz.
+30°C to +55°C	Upper Bandwidth Limit reduced by 2.5 MHz for each °C above 30°C.[a]
Envelope Mode at SEC/DIV settings of 0.5 μs or slower.	Dc to 150 MHz using standard accessory probe, internal 50-Ω termination, or external 50-Ω termination on 1-MΩ input.[a]
−4.7 dB Bandwidth	
Normal or Average Mode. Envelope Mode at SEC/DIV settings of 0.2 μs or faster.	Using 50-Ω external termination on 1-MΩ input.
+30°C to +55°C	Upper Bandwidth Limit reduced by 2.5 MHz for each °C above 30°C.[a]
Single Event Useful Storage Bandwidth	
Normal or Average Mode, SEC/DIV at 0.1 μs or Faster; Repet OFF	DC to 200 MHz (calculated). $USB = \frac{F_{(\text{sample freq max})^c}}{2.5}$
AC Coupled Lower −3 dB Point	
1X Probe	10 Hz or less.[a]
10X Probe	1 Hz or less.[a]
Step Response, Repet and Average On; Average Set to 16	
Rise Time	1.17 ns or less (calculated).[a] $T_r \text{ (in ns)} = \frac{350}{BW \text{ (in MHz)}}$

[a]Performance Requirement not checked in the manual.

[c]Sample freq. max. is 500 MHz.

AutoStep Sequencer (PRGM): With AutoStep, the user can save single front-panel setups or sequences of setups and associated flow control and Input/Output actions for later recall. If MEASURE and/or OUTPUT are saved as part of these setups they can be used for automatic parameter extraction and data printout. 100 to 800 front-panel setups (depending on complexity) can be stored in one or more sequences.

The complete descriptions of these four features are found in Section 5 of the Operators manual included with this instrument.

The following items are standard accessories shipped with the scope instrument:

2	Probe packages
1	Snap-lock accessories pouch
1	Zip-lock accessories pouch
1	Operators manual
1	Programmer's Reference Guide
2	Users Reference Guide
1	Fuse
1	Power cord (installed)
1	Blue plastic CRT filter (installed)
1	Clear plastic CRT filter
1	Front-panel cover

For part numbers and further information about standard accessories and a list of the optional accessories, refer to "Options and Accessories" (Section 7) in this manual. For additional information on accessories and ordering assistance, contact your Tektronix representative or local Tektronix Field Office.

PERFORMANCE CONDITIONS

The following electrical characteristics (Table 1-1) apply when the scope has been calibrated at an ambient temperature between +20°C and +30°C, has had a warmup period of at least 20 minutes and is operating at an ambient temperature between −15°C and +55°C (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

Environmental characteristics are given in Table 1-2. The scope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4. The rackmounted scope meets the vibration and shock requirements of MIL-T-28800C for Type III, Class 5, Style D equipment when mounted using the rackmount rear-support kit supplied with both the 1R Option and the Rackmount Conversion kit.

Mechanical characteristics of the scope are listed in Table 1-3.

Video Option characteristics are given in Table 1-4.

RECOMMENDED ADJUSTMENTS SCHEDULE

For optimum performance to specification, the internal SELF CAL should be done:

1. If the operating temperature is changed by more that 5°C since the last SELF CAL was performed.

2. Immediately before making measurements requiring the highest degree of accuracy.

delay may be set from 1 to 65,536, with a resolution of one event. The DELTA DELAY feature produces two independently settable delayed B Traces in DELAY by TIME.

TRIGGER SYSTEM

The trigger system of the scope provides many features for selecting and processing a signal used in triggering the acquisition system. The conventional features of SOURCE selection, Trigger LEVEL control, Trigger SLOPE, Trigger MODE, and CPLG (coupling) include enhancements not normally found in a conventional oscilloscope.

The choices of VERT, CH1 or CH2, EXT1 or EXT2, LINE, and A*B or WORD (16-bit data word recognition) are available as SOURCE selections for triggering A Horizontal Mode acquisitions. These sources for trigger signals provide a wide range of applications involving specialized triggering requirements. Except for A*B (A AND B) and LINE (power-source frequency), the same Trigger SOURCE selections are available for triggering B acquisitions. The selected trigger signal is conditioned by the choice of input CPLG (coupling). These coupling selections are AC, DC, HF REF, LF REJ, and NOISE REJ. LEVEL control provides a settable amplitude (with CRT readout) at which triggering will occur, and SLOPE control determines on which slope of the triggering signal (plus or minus) the acquisition is triggered.

Trigger MODE choices are AUTO LEVEL, AUTO, NORM, and SINGLE SEQ (single sequence), for the A and A INTENSIFIED Modes, and Triggerable After Delay and Runs After Delay, for the B Mode. AUTO LEVEL provides for automatic leveling on the applied trigger signal. AUTO MODE produces an auto trigger in the event a trigger signal is either not received or not within the limits needed to produce a triggering event. When triggering conditions are met, a normal triggered display results. At SEC/DIV settings of 100 ms per division and longer, the AUTO MODE switches to ROLL. In ROLL MODE, the display is continually updated and trigger signals are disregarded.

NORM (normal) trigger MODE requires that all triggering requirements are met before an acquisition will take place. SINGLE SEQ (single sequence) MODE is a variation of the conventional single-shot displays found on many previous oscilloscopes. In SINGLE SEQ, a single complete acquisition is done on all called-up VERTICAL MODES. Since an acquisition depends on the acquisition mode in effect, many of the scope operating features are altered in SINGLE SEQ. A complete description of this mode is discussed in "Controls, Connectors, and Indicators" in Section 5 of the Operators manual.

The user has a choice of trigger points within the acquired waveform record by selecting the amount of pre-trigger data displayed. The trigger location in the record is selectable from a choice of five pretrigger lengths beginning at one-eighth of the record length and increasing to seven-eighths of the record length. A record trigger position is independently selectable for both A and B acquisitions. Additional trigger positions in the record are selectable via the GPIB interface commands.

CURSOR MEASUREMENTS

Time and Voltage cursors are provided for making parametric measurements on the displayed waveforms. Time may be measured either between the cursor positions (DELTA TIME) or between a selected cursor and the trigger point of an acquired waveform (ABSOLUTE). Time cursor readouts are scaled in seconds, degrees, or percentage values. The 1/TIME cursors may be scaled in hertz (Hz), degrees, or percentage.

Voltage cursor measurements on a waveform display can be selected to read either the voltage difference between the cursor positions or the absolute voltage position of a selected cursor with respect to ground. The volts measurement readouts may be scaled in units of volts, decibels (dB), or percent. The Voltage cursors and Time cursors may also be coupled to track together (V@T and SLOPE) and assigned to a particular waveform for ease in making peak-to-peak and slope waveform measurements. The units for V@T may be volts, percent, or dB; SLOPE may have units of slope (VOLTS/SEC), percent (VOLTS/VOLT), or dB.

WAVEFORM ACQUISITION

Waveforms may be acquired in NORMAL, ENVELOPE, or AVG (Average) acquisition modes; the mode chosen depends on the measurement requirements. NORMAL mode continuously acquires and displays successive acquisitions producing a "live" waveform display similar to that seen with an analog oscilloscope. AVG (averaging) mode averages successive acquisitions of a waveform resulting in an improved signal-to-noise ratio of the displayed waveform. Low-amplitude signals masked by noise become easily visible for making measurements and analysis by averaging from 2 to 256 acquisitions for removing uncorrelated noise. ENVELOPE mode saves the

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found. For maximum input voltage see Table 1-1.

Symbols as Marked on Equipment

DANGER — High voltage.

Protective gound (earth) terminal.

ATTENTION — Refer to manual.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before making any connections to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising from Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for the instrument.

Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the instrument parts list. A replacement fuse must meet the type, voltage rating, and current rating specifications for the fuse that it replaces.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this instrument in an atmosphere of explosive gasses.

Do Not Remove Covers or Panels

To avoid personal injury, the instrument covers or panels should only be removed by qualified service personnel. Do not operate the instrument without covers and panels properly installed.

LIST OF ILLUSTRATIONS (cont)

Page

TABLE OF CONTENTS (cont)

Printed in U.S.A. Specification and price change privileges are reserved.

Instrument Serial Numbers

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000 Tektronix, Inc., Beaverton, Oregon, USA
100000 Tektronix Guernsey, Ltd., Channel Islands
200000 Tektronix United Kingdom, Ltd., London
300000 Sony/Tektronix, Japan
700000 Tektronix Holland, NV, Heerenveen,The Netherlands

THEORY OF OPERATION

SECTION ORGANIZATION

This section of the manual is divided into three subsections, with each subsection increasing in detail. The first subsection is the "Simplified Block Diagram Description" which contains a general summary of instrument operation by diagram. A simplified block diagram accompanies the text. Subsection two is the "Detailed Block Diagram Description" which discusses the circuit functions in greater detail and provides a more in-depth look at the acquisition system. A detailed block diagram is located in the foldout pages at the rear of this manual. Generally, both block diagram descriptions follow the signal-flow path as much as possible and not the schematic diagram number order as is done in the "Detailed Circuit Description".

Subsection three is the "Detailed Circuit Description" which discusses the circuitry shown in the schematic diagram foldouts, also located at the rear of this manual. The schematic diagram number associated with each description is identified in the text and is shown on the block diagrams. For best understanding of the circuit being described, refer to the appropriate schematic diagram and the block diagrams. The order of discussion in the circuit descriptions follows the schematic diagram number order.

INTEGRATED CIRCUIT DESCRIPTIONS

Digital logic circuits perform most of the functions within the instrument. Functions and operation of the logic circuits are shown using logic symbols and terms. Most logic functions are described using the positive-logic convention. Positive logic is a notation system in which the more positive of the two logic levels is the HI (or 1) state; the more negative level is the LO (or 0) state. Voltages that constitute a HI or a LO state vary between specific devices. Refer to the device manufacturer's data book for specific electrical characteristics or logical operation of common parts.

The functioning of linear integrated circuit devices in this section is discussed using waveforms or other techniques such as voltage measurements and simplified diagrams, where required, to illustrate their operation.

SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

This discussion is of the block diagram shown in Figure 3-1.

Attenuators and Preamplifiers (diagram 9)

ATTENUATORS. The Attenuators are settable to 1X, 10X, or 100X attenuation, to reduce the input signal level to within the dynamic range of the Preamplifiers. Input coupling for the signal to the Attenuators may be either AC or DC with 1 MΩ termination or DC with 50 Ω termination. Attenuator and coupling switching are controlled by the System μP using register-activated magnetic-latch switches.

PREAMPLIFIERS. The Preamplifiers provide switchable gain setting and buffering of the attenuated input signal. Single-ended input signals are converted to double-ended (differential) output signals. Variable Vertical Mode gain, vertical position, and DC Balance are controlled by input signals to the Preamplifiers. The System μP-controlled gain in combination with the switchable attenuator settings allow the complete range of available VOLTS/DIV switch settings from 2 mV to 5 V to be obtained. Trigger pickoffs provide a sample of the input signal to the trigger system for use as a triggering signal source. With the Video Option installed, a Channel 2 pickoff signal is supplied from the Preamplifiers as a trigger signal source. Also, a Channel 2 Offset signal used to control the back-porch clamping is provided from the Video Option to the Channel 2 Preamplifier.

Peak Detectors and CCD/Clock Drivers (diagram 10)

PEAK DETECTORS. Additional buffering of the signal to the CCDs is provided by the Peak Detectors for all acquisition modes. The bandwidth of the input amplifiers of the Peak Detectors is switchable for FULL, 100 MHz, and 20 MHz bandwidths. In Envelope acquisition mode, dual min-max Peak Detectors detect and hold the minimum and maximum peak signal amplitudes that occur between sampling clocks. Those min and max signal values are then applied to the CCDs for sampling. Control data from the System μP controls the bandwidth selection, and peak detector clock signals multiplex the signal samples from the Peak Detectors to the CCDs. A calibration signal input is provided to the Peak Detectors for use in automatic calibration and diagnostic testing of the acquisition system.

Common-mode adjust circuitry on the output of the Peak Detectors is used to control the overall gain of the Peak Detector/CCD acquisition subsystem. Using digital signals to the DAC system, analog voltages are generated that set the gain of the Common-mode adjust amplifiers. These amplifiers monitor the dc common-mode level of the Peak Detector outputs and match it to the control gain level set by the System μP. That dc level sets the CCD signal gain.

CCD/CLOCK DRIVERS. The CCDs are fast analog shift registers that can hold more that enough samples to fill the complete waveform record of 1024 samples per channel. The extra samples are used to account for the uncertainty of the trigger point location in the 32 samples stored in the input register. Once a trigger occurs, the samples not needed to fill the waveform records are basically discarded. For fast signals, waveform samples are stored very rapidly and then shifted out at a rate that can be handled by the A/D Converter. When the sample rate is slow enough to allow direct conversion of the input samples, a Short Pipeline mode is used to shift samples directly through the CCD registers. The Clock Driver portion of the devices produces the phase clocks that shift the analog data through the CCD registers. Other clocks used to sample the signal and transfer the samples into and out of the CCD arrays are generated in the CCD Clock and System Clock circuits (diagrams 11 and 7 respectively).

CCD Output (diagram 14)

The differential signals from the four sides of both channels of the CCD arrays are combined and multiplexed onto a single data line to the A/D Converter. The output clocking is referenced to the sample and phase clocks to maintain the correct data timing relationships of the samples. Waveform data samples are therefore stored in the correct Acquisition Memory locations after being digitized.

A/D Converter and Acquisition Latches (diagram 15)

A/D CONVERTER. The combined samples of analog signals are converted to eight-bit data bytes by the A/D Converter. In Envelope Mode, the data bytes are applied to two magnitude comparators, along with the previous maximum and minimum data bytes to determine if it is greater in magnitude than the last maximum or minimum. If a new data byte is greater, the new data byte is latched into the Acquisition Latches; otherwise, latching does not occur. Clocking to direct the signals into the Acquisition

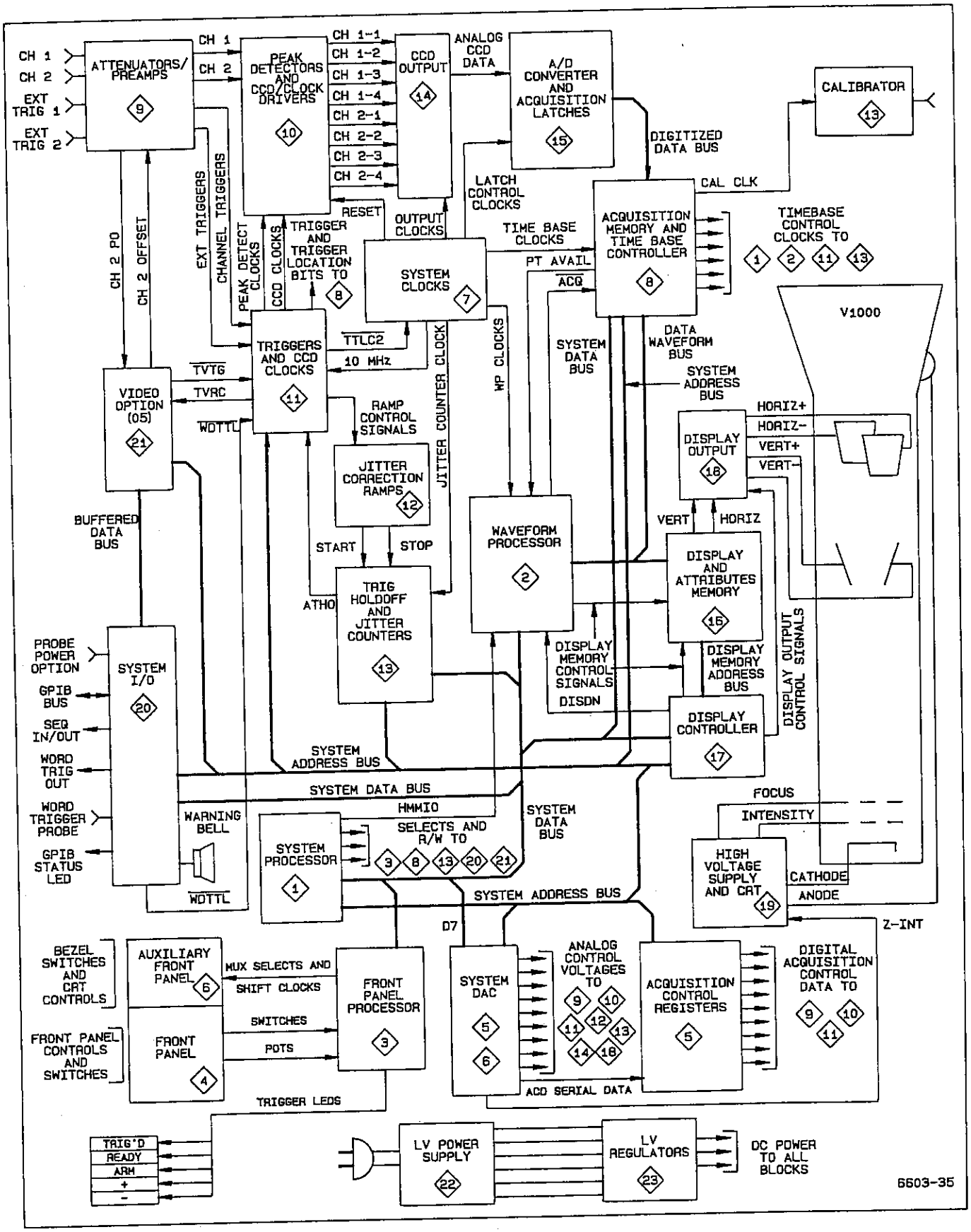


Figure 3-1. Simplified block diagram.

Latches comes from the System Clock circuit and is referenced to the Output Clocks to maintain the correct data input to the magnitude comparators for making the Envelope min-max comparisons.

ACQUISITION LATCHES. For Normal and Average acquisitions, the data bytes are passed directly through the Acquisition Latches to the Acquisition Memory where they are stored temporarily before transfer to Waveform Processor Data Bus and the Waveform Processor Save Memory. The Envelope acquisition waveform bytes in the Acquisition Latches are the maximum and minimum data point values that occurred in the sampling interval. When the SEC/DIV setting reaches the maximum sampling rate, only one min-max pair is present during a sampling interval; and, in that case, the Envelope data byte comparisons are done by a firmware routine as the data is transferred from the Save Memory to the Display Memory.

Time Base Controller and Acquisition Memory (diagram 8)

ACQUISITION MEMORY. Digitized waveform data bytes are transferred from the Acquisition Latches to the Acquisition Memory under control of the Time Base Controller. The data is temporarily stored here before moving to the Waveform Processor Save Memory under control of the Waveform Processor.

TIME BASE CONTROLLER. The Time Base Controller, under direction of the System μP, monitors and controls the acquisition functions. When the pretrigger samples are obtained, the digitization process is started. Samples are counted to store the correct number in the Acquisition Memory, and the trigger point is properly located in the waveform record. Among the various tasks done by the Time Base Controller, Clock signals generated by the Time Base Controller provide the acquisition rate, the calibrator frequency, and enable the Trigger circuitry to accept a trigger after the pretrigger data is acquired.

Waveform Processor (diagram 2)

The Waveform Processor performs the high-speed data-handling operations required to produce and update the CRT displays. Waveform data is transferred from the Acquisition Memory to a "Save" Memory in the Waveform μP work space. Waveforms may be digitally added, multiplied, or averaged, as part of the display processing that the Waveform Processor does before transferring the data to the Display Memory. The Save Memory is kept alive during periods of power-off by the battery-backup system. This back-up system holds the Save waveforms, the reference waveforms and/or front-panel setups for up to three years. The waveform μP memory space and all devices on the Waveform μP address bus are addressable by the System μP via the Bus Connect circuitry for I/O operations.

The Bus Connect circuitry includes logic gating that arbitrates when the Waveform μP memory space (RAM) and addressable devices are under control of the System μP. The System μP may gain control by a BUS REQUEST to which the Waveform μP issues a BUS GRANT signal; or if the Waveform μP is held reset, the System μP issues a BUSTAKE signal. The BUSTAKE is used when the System μP writes a waveform display task list into the Waveform μP Command RAM space. When the reset is then removed from the Waveform μP, it does all the waveform data processing tasks given to it to do by the System μP without further need of System μP action.

Display and Attributes Memory (diagram 16)

The 512 data points to be displayed out of the 1024 data-point record are transferred to the Display Memory from the Waveform μP Save Memory after any required processing such as adding, subtracting, multiplying, or interpolating is done. Subsequent refreshes of the display are then continually made from data stored in the Display Memory, and that memory is only updated as necessary to display different waveforms or portions of the waveform record (a new horizontal position or new waveform called up for display). The Attributes Memory holds all the VOLTS/DIV and SEC/DIV scale factors for each of the waveforms displayed. Readouts of that data are also displayed on the crt.

Display Controller (diagram 17)

The Display Control System controls the display of the waveforms and readouts. Data bytes stored in the Display Memory are read out and D-to-A converted into vertical and horizontal current signals used to generate the waveform dots and readout characters. State-machine circuitry under control of the System μP performs all the display tasks assigned including control of the Z-Axis. The System μP and the Waveform μP are therefore free to carry on with other functions until it becomes necessary to make a display change (such as a menu or display mode change or a waveform data update). Display state-machine clocks are generated from the Time Base Controller 5 MHz clock signal.

Display Output (diagram 18)

Horizontal and vertical signal current from the Display Controller are converted into the deflection voltage signals used to drive the crt deflection plates by the Display Output circuitry. Vector generation circuitry provides a choice of either connected waveform dots (vectors on) or a dots-only waveform display. Display switching circuitry connects the correct deflection signals to the vertical and horizontal output amplifier for YT (vertical signal versus time), XY (horizontal signal versus versus vertical signal), or readout data. Dynamic offset correction of the vertical and horizontal output amplifiers is provided that minimizes trace shift due to intensity changes.

System Processor (diagram 1)

The System μP, under program direction, controls all the functions of the scope and coordinates the functions of the two other microprocessors (the Front-Panel μP and the Waveform μP). The System μP has a 16-bit address bus and a separate 8-bit data bus. No multiplexing of the data bus is required. Addresses are decoded to access the memory-mapped devices on the data bus, and control signals generated by the System μP control communication between the μP and the bus devices. An extensive interrupt circuit enables devices on the bus to request servicing when necessary to get new instructions or take other action. A power-up reset circuit permits an orderly power-on and power-off sequence of the System μP.

Permanent programming used to control the Operating System resides in the System ROM. The System ROM contains one 16K byte × 8-bit memory device and four 64K byte × 8-bit memory devices for a total of 272K bytes of memory. A page-switching scheme is used to permit the System μP to access all the available memory addresses of ROM.

System RAM consists of a single 32K byte × 8-bit memory device. Data needing short-term storage (data used for performing various control functions) as well as data needing long-term storage (calibration constants, the front-panel setup at power down, etc.) are stored in this nonvolatile RAM. A battery-backup system maintains the data in this memory during power off.

NOTE

Although all the data in this memory device is backed up and is, therefore, nonvolatile, that part of the System RAM reserved for data that NEEDS to be backed up is referred to as NVRAM throughout this section. Parts of System RAM that do NOT NEED backing up are referred to as volatile RAM or just RAM.

Front Panel Processor (diagram 3)

The Front Panel μP is a special-purpose device used to respond to switch and control changes. When a control changes, the Front Panel μP informs the System μP so that the operating state may be altered to match the requested change. Potentiometer controls are digitized to provide the necessary change data to the System μP. The System μP notes the control that changed, the amount and direction of change (if a pot), and sends out the necessary commands to make the change. New settings are updated in the nonvolatile RAM so that they will be available in the event of a power-off. On a power-on, the Front-Panel μP receives instructions as to how the switches are to be interpreted and then begins scanning the front panel, watching for a control to change. The System μP is then free to carry on with other functions.

Front Panel (diagram 4) and Auxiliary Front Panel (diagram 6)

All the buttons and knobs of the Front Panel and Auxiliary Front Panel are "soft" controls and do not directly activate a circuit function. This fact allows the switch functions and menu labels to be changed (especially the bezel buttons of the Auxiliary Front Panel which are used to make menu selections) as necessary. Buttons may be defined by the System μP to be push-push on-off, momentary contact, continuous, or toggle switches. Control changes are monitored by the Front Panel μP. Potentiometer controls are digitized; and when a change occurs, the amount and direction of change is sent to the System μP to make the appropriate operational changes. Push buttons that are pressed are interpreted as to what type of switch action occurred (from the switch-type definition list) and that information is sent to the System μP to make the appropriate operational changes.

All the buttons and knobs located to the right of the crt (facing the scope) are monitored via circuitry of the Front Panel. The Auxiliary Front Panel contains the circuitry required to monitor the bezel buttons (menu selection buttons), the push buttons, and the INTENSITY knob (all located directly beneath the crt). Probe coding for the vertical-channel and external-trigger BNC connectors and the 50 Ω overload circuits for CH 1 and CH 2 are also monitored via the Auxiliary Front Panel circuitry.

System DAC (diagrams 5 and 6)

The System DAC is used in normal operation to set the various analog control voltages throughout the instrument. Such things as preamplifier gain, vertical position and centering, trigger levels, holdoff time, common-mode adjust, scale illumination, intensity of the various CRT displays, and CCD positions offsets are all controlled by the System μP via the System DAC. Digital values representing the analog voltage levels required for the various controls are written to the digital-to-analog converter (DAC) input registers where they are converted to analog voltage levels at the inputs to the Sample-and-Hold circuits. The Sample-and-Hold circuits maintain a fixed output voltage to the controlled circuit between updates by the System μP.

For calibration and diagnostic purposes, the System DAC is used to send known voltage levels to various circuits. Those levels may then be adjusted to remove offsets and set gain levels to achieve analog calibration or to test the gains and offsets for diagnostic purposes.

Acquisition Control Registers (diagram 5)

The Acquisition Control Registers are the digital control interface between the System μP and the switchable acquisition circuitry. Switching data is written to the

Registers to control the setup of the Peak Detectors, the A/B Trigger Generator, the Trigger Logic Array, and the Phase Clock Array. Additional decoding circuitry produces clocking signals used to load controlling data into Attenuator Register, the CH1 and CH2 Preamplifiers, and the A/B Trigger Generator.

Triggers and CCD Clocks (diagram 11)

TRIGGERS. The Trigger circuits detect when a trigger meeting the setup conditions occurs. Triggering signals are selectable by the A/B Trigger Generator from a choice of the following sources: CH 1, CH 2, EXT 1, EXT 2, and LINE. The Trigger Logic Array makes possible the further choices of TV Trigger ($\overline{\text{TVTG}}$), WORD Trigger ($\overline{\text{WDTTL}}$), or A and B Trigger. Upon receiving a valid trigger, the acquisition in progress is allowed to complete. Conditions for triggering, such as Level, Slope, Coupling, and Mode, are determined by the A/B Trigger Generator. Other triggering conditions such as delay by time, delay by events, and A and B Trigger are decided by the Trigger Logic Array which produces the output gates signaling a trigger event. The System μP sets up the operating modes for the A/B Trigger Generator and the Trigger Logic Array via the Acquisition Control Registers (diagram 5). Control signals to the Jitter Correction Ramps (RAMP and $\overline{\text{RAMP}}$) are generated by the Trigger Logic Array to start measuring the time between the sample clock and the trigger event. That time difference is used to correctly place the samples when repetitive sampling is used.

CCD CLOCKS. The CCD Clocks (used to move data into and out of the CCDs), the Peak Detector Clocks, the ramp-switching signals to the Jitter Correction Ramp circuits, and the trigger location bits (needed to place the trigger position with respect to the waveform data) are all generated by the Phase Clock Array. A master clock signal of 500 MHz is generated by the Phase-Locked Loop circuit and voltage-controlled oscillator. The master clock frequency needed is determined by the sampling rate at a particular SEC/DIV switch setting. Frequency dividers in the Phase Clock Array reduce the master clock frequency to the lower rates of the output clocks as determined by the System μP via the Acquisition Control Registers (diagram 5).

Jitter Correction Ramps (diagram 12)

The Jitter Corrections Ramps work in conjunction with the Jitter Counters to detect and measure the time difference between a trigger event (that occurs randomly) and the sample clock. That time difference is used to correctly place sampled data points into the waveform record when those samples are acquired on different triggers (repetitive sampling). Two ramp generators are used, so two time measurements are made. The System μP will determine which measurement is the one actually used. The RAMP and $\overline{\text{RAMP}}$ signals from the Trigger circuits control the start and stop of the ramp signals while the SLRMP1 and SLRMP2 signals control switching between the fast-charging current source and slow-discharging current source. Since the SLRMP signals are related to the sample clock, the amount of charge stored from the fast-charging current source before switching to the slow ramp occurs is a measure of the time difference between the trigger and the sample clock. The Jitter Counters start counting when the SLRMP signal switches to the slow ramp, and they are stopped when a comparator circuit determines that the ramp level has discharged to a fixed reference level.

Trigger Holdoff and Jitter Counters (diagram 13)

TRIGGER HOLDOFF. The A Trigger Holdoff circuit prevents the A/B Trigger Generator (diagram 11) from recognizing a new trigger event for a certain amount of delay time after an acquisition has been completed. The delay allows all of the data handling of the acquired samples to be completed before starting a new waveform acquisition. Minimum holdoff time is dictated by the SEC/DIV switch setting. A front-panel HOLDOFF control permits the user to increase the holdoff time as an aid in improving triggering stability on certain signals.

JITTER COUNTERS. The Jitter Counters (one for RAMP1 and one for RAMP2) start counting the 40 MHz clock when a START signal is received from the Jitter Counter Ramps switching circuit. That start occurs at the beginning of the slow ramp discharge. When the level of the slow ramp decreases to the fixed reference level, a STOP signal generated by a comparator in the Jitter Counter Ramps circuit halts the count. The 8-bit count bytes held in the Jitter Counters are then read by the System μP via address-selected bus buffers as two measures of the time difference between the trigger point and the sample clock. Since the timing between the two ramps is not identical (but both times are referenced), one measurement may have been made with better slope characteristics than the other (over a more linear portion of the discharge curve). The count producing the least ambiguity is used by the System μP to correctly position the waveform samples in the memory when repetitive sampling is done.

Calibrator (diagram 13)

The Calibrator circuitry shapes the CALCLK signal from the Time Base Controller to produce a signal with a faster rise and fall time and very precise amplitude. Frequency of the Calibrator signals changes (within limits) as the SEC/DIV switch changes. Signal amplitude is 400 mV (starting from zero), and the effective output impedance is 50 Ω.

System Clocks (diagram 7)

The System Clocks circuitry produces the fixed-frequency clock signals used throughout the scope. A 40 MHz crystal-controlled oscillator circuit produces the master clock signal that is divided down to provide the various system clocks that are needed. Some of the special clocks generated are the CCD Data Clocks, used primarily to switch the analog signal samples from the CCDs to the input of the A/D Converter and switch the converted data bytes to the Acquisition Latches. The reference frequency (10 MHz) to the Phase Clock Array in the CCD Clock circuitry (diagram 11) is also selected by the System Clocks circuitry. A Secondary Clock Generator state-machine circuit produces three clocking signals to the Waveform μP to control the activity of that device.

High Voltage and CRT (diagram 19)

The High Voltage and CRT circuitry provides the auxiliary voltages needed by the CRT to produce a display. Focus, intensity, trace rotation, astigmatism, geometry, Y-Axis alignment, heater, and cathode-to-anode accelerating voltage are all provided by the various circuits included. These circuits are: the High Voltage Oscillator, the High Voltage Regulator, the +61 V Supply, the Cathode Supply, the Anode Multiplier, the DC Restorer, the Focus and Z-Axis Amplifiers, the Auto Focus Buffer, and the various crt adjustment potentiometers.

System I/O (diagram 20)

The System I/O circuits provide the interfaces between the scope and external devices that may be connected. Included in the interfaces is a standard general-purpose interface bus (GPIB) that permits two-way communication between the System μP and a GPIB controller or other IEEE 488-1980 compatible GPIB devices. The GPIB interface permits waveforms, front-panel setups, and other commands or messages to be both sent and received by the scope.

A second interface is the Word Trigger circuitry used to control the word recognization patterns of the optional Word Recognizer probe. All firmware and hardware (including connectors) required for use of the Word Recognizer probe is supplied as standard equipment. A trigger produced by the probe ($\overline{\text{WDTTL}}$) may be internally selected to trigger the scope, and it may be supplied to an external device via the WORD TRIG OUT connector on the rear panel.

Three BNC connectors comprise a third interface which is used to help control the AutoStep Sequencer. SEQUENCE IN is an input that accepts TTL-compatible signals for starting a sequence and stepping a paused sequence. SEQUENCE OUT is an output that issues a TTL-compatible signal upon the completion of a sequence. STEP COMPLETE issues a TTL-compatible signal to indicate when a step in sequence is complete.

Probe power connectors are an option for supplying the power requirement of active Tektronix probes. The option consists of two probe power connectors installed on the rear panel of the scope.

An audible alarm bell is provided to give the user warning of events that may require attention. GPIB errors are typical events that produce the warning bell so that a user may take notice of the error event. Another instance that causes the warning bell is an attempted call-up of an invalid operating condition from either the front panel or the GPIB. Typically, warning and error messages are also displayed on the crt to aid the user in determining the nature of the problem.

Video Option (diagram 21)

The Video Option (Option 05) consists of additional installed hardware that enhances triggering on and viewing of composite video signals. Option 05 circuitry contains both Video Processing and Trigger Generation circuitry. Video Processing stabilizes the input signal and separates the video sync signals (horizontal and vertical sync pulses) from the video signal. A wide range of video signal levels are accommodated by using automatic gain control of the amplifier that sets the level into the sync separator. Separated sync pulses are counted to permit the user to select the line number that will produce a trigger event. Back-porch clamping is available for the Channel 2 display, and when used, it removes or reduces the level of power-supply hum that may be accompanying the composite video signal display.

Low Voltage Power Supply (diagram 22)

The majority of the low voltages required to power the scope are produced by a high-efficiency, switching power supply. Input ac power of either 115 V or 230 V within the frequency range of 48 Hz to 400 Hz is rectified and used to drive a switching circuit at a frequency of about 50 kHz. A smaller power transformer is possible with the higher

frequency switching, and much more efficient power transfer is possible. Regulation of the power to the switching transformer is controlled by a pulse-width modulator (PWM) using feedback from one of the rectifier transformer outputs. The PWM controls the on-time of the switching transistors that deliver energy to the transformer primary winding. If the feedback voltage is too low, more energy is supplied by turning on the switching transistors longer. Automatic overvoltage and overcurrent sensing circuits shut down the switching if either type of overload occurs. The ac input has an interference filter, primary line fusing, and a thermal cutout that shuts down the power supply in the event of overheating.

Low Voltage Regulators (diagram 23)

The Low Voltage Regulators remove ac noise and ripple from the rectified output voltages from the power transformer. Each regulator automatically current limits the output and prevents the current from exceeding the normal power limits. This limiting prevents further possible damage to the power supply or other scope circuitry. Each of the power supply regulators controls its output voltage level by comparing the output to a known voltage reference level. To maintain stable and well-regulated output voltages, highly stable reference voltages are developed for making the comparisons.

DETAILED BLOCK DIAGRAM DESCRIPTION

INTRODUCTION

This description of the Detailed Block Diagram (found in the "Diagrams" section of this manual) provides an overview of the operation of many of the circuits and their functions. The emphasis is on the acquisition system, and a "signal flow" approach is used as much as possible. No attempt is made in this discussion to specifically cover all the circuitry shown on the block diagram, though most is covered in general as it relates to those areas described in detail. The components discussed for each schematic diagram are generally outlined in functional blocks on their corresponding schematic diagram. These "function blocks" also appear on the "Detailed Block Diagram" within outlined areas that correspond to the schematic diagrams. Refer to both the Detailed Block Diagram and the Schematic Diagrams as needed while reading the following description.

INPUT SIGNAL CONDITIONING AND ANALOG SAMPLING

Signals applied to the CH 1 and CH 2 input connectors are coupled to their respective attenuators. The CH 1 and CH 2 attenuators (diagram 9) are settable for 1X, 10X, and 100X attenuation, with input-coupling mode choices of AC, DC, and GND. Input termination resistance of either 1 MΩ or 50 Ω is selectable with the DC input coupling choice. The attenuation factor, input coupling mode, and input termination settings for each input are controlled by the System μP (diagram 1) through the Attenuator Control Register (diagram 9), based on the Front Panel control settings chosen by the user.

The attenuated CH 1 and CH 2 signals are buffered by their respective Preamps (diagram 9) before they are passed on to the Peak Detectors. Preamplifier gain is controlled by the System μP using a serial control-data line via the Miscellaneous Register (diagram 1) and the DAC MUX (digital-to-analog converter multiplexer) Select circuit. Serial data is clocked into the internal register of the Preamps via the Control Register Clock Decoder (diagram 5). As with the attenuator settings, the gain-setting data output by the System μP depends on the user-selected Front Panel control settings. The range of attenuation settings coupled with the gain-control settings of the Preamps allows the complete range of available VOLTS/DIV switch settings (from 2 mV to 5 V) to be obtained.

In addition to signal gain and input signal buffering, the Preamps convert the single-ended input signal to a double-ended differential output signal that improves the common-mode rejection ratio. Input ports used to control the DC Balance, the Variable VOLTS/DIV gain, and the Vertical Position are provided in the Preamp stages. Analog control voltages to these inputs are developed by the System DAC and routed to the Preamps via the DAC MUX/0 Sample-and-Hold circuit (diagram 5). Trigger pickoff circuits in each Preamp provide a sample of the vertical signal that may be selected by the Trigger circuitry as the trigger signal source.

The differential output signals from the Preamps are applied to their corresponding Peak Detector. Input amplifiers within the CH 1 and CH 2 Peak Detectors (diagram 10) buffer the applied signals and provide a constant input resistance of about 75 Ω to those signals. The

buffered signals are then either amplified further or "peak detected" and amplified, depending on the acquisition mode setting.

The System μP controls the operating mode of the Peak Detectors via control data writes to the Acquisition Control Registers (diagram 5). Some of the resulting digital outputs drive control inputs on the Peak Detectors, while others control the enabling and disabling of the Peak Detector clock signals from the CCD (charge-coupled device) Phase Clock Generator (diagram 11). The effect of this combined action depends on the acquisition mode selected. For NORMAL and AVG (average) acquisition modes, the peak-detect function of the Peak Detectors is disabled and the input signals are only amplified for application to the CCDs. For ENVELOPE mode, however, the peak-detect portion of the internal circuitry is enabled, and the maximum and minimum signal amplitude levels that occur during a sampling interval are detected. Those maximum and minimum values are then amplified and passed on to the CCDs.

Other inputs to the Peak Detectors control the input amplifier Bandwidth Limit setting (FULL, 100 MHz, or 20 MHz) and provide for the application of the calibration signal used for instrument calibration and self diagnostics. Calibration voltage levels applied to the Peak Detectors are generated by the System μP via the System DAC (diagram 5), DAC MUX 3, and the Cal Ampl circuit (diagram 6). The System μP selects between either the normal signal inputs or the calibration signal inputs using data written to the Acquisition Control Registers. The bandwidth of the input amplifiers of the Peak Detectors is also controlled via the Acquisition Control Registers, based on the user-selected Bandwidth Limit setting.

The signal-sampling process of CCDs (diagram 10) requires that four differential-signal pairs be available from each Peak Detector. Each CCD will use two or four of the output pairs as input signals, depending on the analog sampling mode. Briefly, the FISO sampling mode (fast-in, slow-out) requires 1088 samples to be shifted into each CCD. Clocking is such that each of the four sides of the CCD receives one-quarter of the required samples (272) on one of four synchronized clocks of the same frequency (62.5 MHz) but different phase (each lags its predecessor by 90 degrees). The first pair of differential outputs are shifted into a pair of internal registers in one side of the CCD. Each of three remaining pairs of differential output signals is identical to the first pair, and each pair is shifted into two registers corresponding to its CCD side. Since, as mentioned, each CCD side is clocked at 62.5 MHz, but receives its samples on clocks (90 degrees) out-of-phase, a maximum sampling rate of 250 megasamples per second is produced using only a 16 ns clocking rate. A second sampling method, called the "Short-Pipeline" mode, uses only two sides of each CCD and samples only two of the output signal pairs from the Peak Detectors. FISO and Short-Pipeline analog sampling modes are both discussed later in this description and in the "Time Base Controller and Acquisition Memory" portion of the Detailed Circuit Description.

The Common-Mode Adjust circuits (U540A, B, C, and D, and associated components) vary, under control of the System μP, the common-mode voltage levels at the output of the Peak Detectors. These voltages are adjusted at instrument calibration to optimize CCD operation.

The common-mode adjusted signal pairs (two per Peak Detector) are applied to their corresponding side of the CCDs. There, they are analog sampled. The process consists of converting the analog voltages into individual, charged "packets" having a charge directly related to the voltage amplitude of the signal sample.

At SEC/DIV settings of 50 μs and faster, the signals are sampled at a faster rate than the maximum conversion rate of the A/D Converter. This mode is the "fast-in, slow-out" (FISO) sampling mode. When enough samples have been stored in the parallel register array of the CCDs to fill a waveform record after a trigger event, sampling stops (fast-in). The stored analog samples are then clocked out of the CCD arrays at a rate that the A/D Converter can handle (hence, slow-out). For SEC/DIV settings slower than 50 μs, the Short-Pipeline sampling mode is used. In Short-Pipeline, the acquisition rates are slower than the maximum digitizing rate of the A/D Converter. Samples are taken at a constant rate in Short-Pipeline mode, but to account for the slower acquisition rates needed for each successively slower SEC/DIV setting (from 100 μs to 5 s), samples that are not needed are ignored. Short-Pipeline mode is so named because the samples do not fill all of the parallel registers within the CCDs, but take a "short" serial path through the CCDs (see the "Detailed Circuit Description" for more information).

Analog samples are continually clocked into the CCDs by the output clocks of the CCD Phase Clock Array until a valid trigger is recognized by the Acquisition System. The Time Base Controller (diagram 8) provides the reference frequency to the CCD Phase Clock Array via the Reference Frequency Selector and the Phase-Locked Loop circuit (diagram 11). Dividers in the CCD Phase Clock Array synthesize the clocking frequencies needed for saving the acquisition at the different SEC/DIV settings. The Time Base Controller also controls the acquisition mode (FISO, Short-Pipeline, or ROLL) and the storing of acquired samples into the Acquisition Memory.

At this point in the sampling process the Time Base Controller is waiting for a triggering gate from the Trigger System to complete the acquisition (see "Acquisition Process and Control"). Extra pretrigger samples acquired while waiting for a trigger will either be flushed out of the output wells of the CCDs (FISO mode) or converted and stored in the circular Acquisition Memory (diagram 8), but not moved to the Save Memory (Short-Pipeline mode). The exception to this is ROLL mode; a trigger event is not required for ROLL acquisitions. Digitized data is moved through the Acquisition System to continually update the display with each waveform data point acquired.

ACQUISITION PROCESS AND CONTROL

To do a waveform acquisition, the System μP addresses the internal instruction registers within the Time Base Controller and then writes the setup data into the registers. The setup data defines the acquisition mode (FISO, Short-Pipeline, or ROLL), the time base clocking rate (for the SEC/DIV setting), the trigger position, and other instructions for how an acquisition is to be made.

Once the setup data is in the Time Base Controller instruction registers, the System μP generates a strobe that starts the acquisition and turns control of the Acquisition System over to the Time Base Controller. The Time Base Controller then begins monitoring the CCD Phase Clocks to determine when an adequate number of analog samples are in the CCDs to fill the pretrigger requirements. When those samples have been obtained, the Time Base Controller enables the Trigger Logic Array (diagram 11) to accept a trigger and begins looking for a triggering gate from the Trigger Logic Array (via the CCD Phase Clock Array). This waiting period is the continuous analog sampling state for the CCDs referred to at the end of the "Input Signal Conditioning and Analog Sampling" discussion.

With the Trigger System enabled, the A/B Trigger Generator (diagram 11) monitors the selected source for a signal that meets the analog triggering criteria. Source selection and triggering criteria are controlled by serial data writes from the System μP (via the Data MUX Select circuit) based on the Front Panel settings selected by the user. When the analog triggering conditions are met, the A/B Trigger Generator gates the Trigger Logic Array. Once enabled, the Trigger Logic Array monitors other triggering criteria (Trigger Mode, Delay Time setting, Hold Off timing, etc.) to determine the actual "Record" trigger point in the waveform data record. The System μP writes data control bits defining the Trigger Logic Array operating mode to the internal registers of the Trigger Logic Array via the Acquisition Control Registers.

When the Trigger Logic Array determines that the additional triggering conditions are also met, the Time Base Controller is gated (via the CCD Phase Clock Array), and the post-trigger samples are taken (if required) to finish the acquisition. How the acquisition is completed after the trigger point is determined, depends on the analog sampling mode in effect.

FISO Mode

For FISO mode, the CH 1 and CH 2 CCDs must each hold 1024 samples (plus some extra samples used in locating the correct trigger point). After the trigger event, the Time Base Controller counts a sampling clock from the CCD Phase Clock Generator to determine when enough post-trigger samples have been shifted into the CCDs to finish the acquisition. When the record is filled, the analog sampling process is stopped by disabling the sampling clocks output by the CCD Phase Clock Generator. Converting the stored analog information into digital data and saving it into the Acquisition Memory is then started. Both the "conversion" and "save" aspects of the acquisition process are discussed in "Analog Data Conditioning and A/D Conversion" and "Acquisition Processing and Display."

Short-Pipeline Mode

For Short-Pipeline acquisitions, each CCD can contain only 37 samples before the "pipe" is full. This means that samples must be continuously shifted through the digitizing process and into Acquisition memory as the samples are being taken. Since the pretrigger and post-trigger distribution of the data in the acquisition record is not defined until a trigger occurs, converted data is continually stored in the Acquisition Memory. If the Acquisition Memory space should become filled before a trigger occurs, newly acquired data will simply displace the old in a circular manner (oldest data replaced first). After a trigger, the Time Base Controller counts another sampling clock to determine when enough samples have been moved into the Acquisition Memory to satisfy the post-trigger requirements and then turns the Acquisition Memory space over to the Waveform μP. The Waveform μP transfers the samples into the Save Memory for eventual display.

DATA CLOCKING TO ACQUISITION MEMORY

FISO Mode

In FISO mode, the Time Base Controller signals the CCD Phase Clock Array (U470, diagram 11) to begin clocking waveform samples out of the CCDs. The Time Base Controller monitors the Trigger Location signals from the CCD Phase Clock Array to determine precisely where in the acquisition the trigger occurred. When the samples

not needed to fill the 1024-point waveform record have been clocked out so that only the samples properly positioned around the trigger point remain in the CCD, the Time Base Controller enables the save acquisition clocking to begin moving the digitized samples from the A/D Converter into the Acquisition Memory, thus saving the waveform record. (See "Detailed Circuit Description" for more trigger point location information.)

To do a waveform save, the Time Base Controller is selected to control writing into the Acquisition Memory via the Memory Mode Control circuit (diagram 8). The $\overline{\text{SAVEACQ}}$ clock circuitry is then enabled to pass a 4 MHz clock signal ($\overline{\text{SHIFTD200N}}$) from the CCD Data Clock circuit (diagram 7) to do the memory writes at the FISO rate.

The memory write clock also increments the Acquisition Memory Address Counter to provide the address for writing the next data point into the Acquisition Memory. The address is latched into the Record-End Latch during each memory write so that the beginning of the acquisition record can be determined when the Acquisition Memory is accessed later.

As the samples are being moved into the Acquisition Memory, the Time Base Controller monitors clocks from the CCD Data Clock circuit to determine when the 1024 digitized samples (per each channel) are saved. The Time Base Controller then stops writing to the Acquisition Memory by disabling the write clock and switches control of the memory to the Waveform μP (again, via the Memory Mode Control circuit). The Time Base Controller then strobes the Waveform μP (diagram 2) to signal that the acquisition is complete and the waveform data is available for processing and display.

Short-Pipeline Mode

For Short-Pipeline mode, the Time Base Controller generates an enabling clock that controls the 2 MHz write clock to the Acquisition Memory. The correct enabling rate of the $\overline{\text{SAVEACQ}}$ write clock for the selected SEC/DIV setting is synthesized within the Time Base Controller, using a CCD Data Clock input to obtain the base frequency. This enabling clock turns on the controlling gate circuit to pass only two $\overline{\text{SAVEACQ}}$ clocks (via the Mode Control Circuit) to write to the Acquisition Memory, saving one digitized data point per channel (two in Envelope Mode—one max and one min per channel). Then the synthesized clock from the Time Base Controller disables the $\overline{\text{SAVEACQ}}$ clock for a certain number of clock cycles. Specifically, the number of ungated clock cycles equals the SEC/DIV setting divided by 50 μs, i.e., four clock cycles at a SEC/DIV setting of 200 μs. Therefore, the samples saved in the Acquisition Memory in Short-Pipeline mode produce a constant 50 samples per horizontal division when displayed, regardless of the SEC/DIV setting.

The remainder of the Short-Pipeline save operation is similar to a FISO save. The Acquisition Memory Address Counter is incremented by the clock that writes data to the memory as in FISO, but at the synthesized rate rather than at the 4 MHz FISO rate. As in FISO, the Trigger Location information is used to determine the trigger point location. Enough samples are saved into memory after the trigger point is found to fill the post-trigger requirements before turning control over to the Waveform μP.

ANALOG DATA CONDITIONING AND A/D CONVERSION

All four pairs of the differential output signals from the CH 1 and CH 2 CCDs are applied to the inputs of the corresponding pairs of Gain-Cell amplifiers (diagrams 14 and 14a). Each amplifier (there are two Gain-Cell amplifiers on each of the four Gain-Cell boards) converts the differential signal clocked to its inputs to a single-ended output signal. That signal is used to drive the input of a corresponding Sample-and-Hold circuit (also shown on diagram 14).

The CCD Data Clocks and the CCD Output Sample Clocks (diagram 7) control the timing between when the signals are coupled to their corresponding Sample-and-Hold circuits and when the Sample-and-Hold circuit outputs are coupled to the single analog input of the A/D Converter (diagram 15). Briefly for FISO mode, the timing is as follows:

1. A CCD Output Sample clock gates the outputs of all four CH 1 Gain-Cell amplifiers to the input of their associated Sample-and-Hold circuit. There, the input levels are sampled, and the gating is then disabled to hold the sampled level on the Hold capacitors. One of the CH 1 Sample-and-Hold output circuits is then gated on to pass the sample level to the A/D Converter for digitization.

2. While the output level of the first CH 1 Sample-and-Hold is gated to the A/D Converter, a CCD Output Sample clock gates the outputs of all four CH 2 Gain-Cell amplifiers to their corresponding CH 2 Sample-and-Hold circuits. Both the first CH 1 Sample-and-Hold outputs and the inputs to the CH 2 Sample-and-Hold circuit are then ungated, and the first CH 2 Sample-and-Hold output circuit is gated on to pass its held signal level to the A/D Converter.

3. The first CH 2 output is then ungated, and the second CH 1 Sample-and-Hold output and the second CH 2 Sample-and-Hold output are gated on in succession to couple their held levels to the A/D Converter. This multiplexing process continues until the third and fourth

Sample-and-Hold outputs of both CH 1 an CH2 are gated in turn to the A/D Converter. The cycle then repeats until 1024 samples from all four sides of both CCDs have been converted.

NOTE

The samples are clocked through each side of the CCD at a 500 kHz rate, resulting in an output sampling rate of 2 MHz per channel. Also note that the 8-to-1 gating of the two channels and their respective outputs results in a 4 MHz time-multiplexed (8-to-1) signal to the A/D Converter.

For Short-Pipeline sampling mode, the gating for the inputs to the Sample-and-Hold circuits is the same as in FISO mode. However, since only one side of each CCD is used per channel, only one pair of differential outputs (per CCD) and the corresponding Gain-Cell amplifier and Sample-and-Hold circuits transfers valid waveform samples to the A/D Converter. The Short-Pipeline mode save-acquisition clocking ensures that only the valid converted data is saved (see "Short-Pipeline Mode" in "Acquisition Process and Control"). Observe, however, that the signal to the A/D Converter is still a 4 MHz time-multiplexed signal, but with invalid data half of the time. Since the invalid data is, in effect, discarded by the Short-Pipeline Mode save-acquisition clocking, the A/D Converter continues to operate at a constant 4 MHz conversion rate as in FISO mode.

The time-multiplexed signal is applied to the input of the A/D Converter circuit for digitization. The System Clocks circuit (diagram 7) provides a 4 MHz clock to the converter, for a 4 MHz data-conversion rate of the input signal. The resulting digital output byte is applied in four 8-bit bytes to the Acquisition Latches (diagram 15).

For Normal and Average Acquisition Modes, data is clocked into the Acquisition Latches by another 4 MHz clock time-shifted from the 4 MHz clock used by the A/D Converter. Enabling of the outputs of the Acquisition Latches is controlled by the CCD Data clocks in a sequence that ensures that the data clocked out from the enabled latch corresponds to the CCD side and Sample-and-Hold circuit that provided it. The 8-bit sample bytes are then saved in Acquisition memory in the same order they were obtained. This "structured" method for saving acquisitions keeps the data in the correct time sequence for display.

For Envelope Mode, the Time Base Controller disables continuous gating of the 4 MHz clock to the Acquisition Latches. This action turns over the gating of that clock to the Envelope Min-Max Comparators (diagram 15). With the 4 MHz clock ungated, the CCD Data Clocks will continue to control the enabling of the outputs of the acquisition latches as described, but the new data bytes are not continually clocked into the latches. The result is that only the data bytes clocked in by the Envelope Min-Max Comparators are sequentially clocked to the Envelope Data bus in the following manner: CH 1 max, CH 2 max, CH 1 min, CH 2 min. This is the same order in which the analog samples are clocked into the A/D Converter.

The output of the A/D Converter is fed to the Envelope Min-Max Comparators (diagram 15). The outputs of the Acquisition Latches are also fed back to those comparators. Due to the previously described timing action of the CCD Data Clocks, the newly digitized minimum or maximum value from the Peak Detectors (see "Input Signal Conditioning and Analog Sampling") is compared to the last value latched into the Acquisition Latch that corresponds to the new point. If the newly acquired point is outside the previous min or max value, the appropriate Envelope Min-Max Comparator gates the 4 MHz clock, and the new data byte is latched into the corresponding acquisition latch.

ACQUISITION PROCESSING AND DISPLAY

Data Transfer to SAVE Memory

Once the 1024 digitized signal bytes per channel are in Acquisition Memory, the Time Base Controller ungates the SAVEACQ clock and switches the the Memory Mode Control circuit to the Waveform μP. It also signals the Waveform μP, via the Display Status Buffer (diagram 2), that the acquisition is complete. The Waveform μP can then access the Acquisition Memory.

When the Waveform μP reads the acquisition done (ACQDN) signal from the Time Base Controller, it writes an address (via the Address Latch) which is decoded by the Register Address Decoding circuit (diagram 2). The decoded address signals the Record-End Latch (diagram 8) to enable its contents (the last addressed memory location for the stored acquisition) to the Waveform μP data bus to be read to determine the location of the last record byte stored. The Waveform μP then uses that location to determine the location of any byte in Acquisition Memory.

The Waveform μP outputs (via its Address Latch) addresses to the Address Counter for Acquisition Memory. The Address Counter is held in its load mode by the Waveform μP (via the Memory Mode Control circuit), passing the address through to Acquisition Memory. The Waveform μP enables the Acquisition Memory and provides the clocks (via the Memory Mode Control circuit)

to move stored data out to the Waveform Data bus via the Data Bus buffer. This data is written either into the Waveform Save Memory or into an internal register of the Waveform μP for processing, depending on the display requirements.

Most transfers from Acquisition Memory are straight out of Acquisition Memory, through the Waveform Data Buffer, and into a corresponding memory location in Waveform Save Memory. However, the Waveform μP sometimes disables the Waveform Data Buffer and reads the data directly into its own internal register via the Data Bus Buffer. The Waveform μP then processes it according to tasks assigned by the System μP, using routines stored in its own ROM. For instance, in Envelope mode the Waveform μP will read (into a second internal register) the corresponding byte stored in Waveform Save Memory from the previous acquisition. If the new byte, stored in the first internal register, is determined to be a new max or min value, the Waveform μP uses it to replace the previous value in Waveform Save Memory.

It should be noted that the Waveform Save Memory is a paged RAM memory. The Waveform μP uses a paged address scheme to load waveform data into one of six possible sections, depending on the source (CH 1 or CH 2) or the destination (REF1, REF2, etc) of the waveform. Observe also that the Waveform Save Memory RAMs are supplied power by the Standby Circuit when instrument power is off, allowing for preservation of the waveform data stored in each of the six sections. See the "Detailed Circuit Description" for more information concerning the structuring of the Waveform Save Memory and operation of the Standby Power circuit.

Data Transfer to Display Memory

Once an acquisition is stored in the Waveform Save Memory, it must be moved to the proper locations in Display Memory, from where it is converted back to an analog signal for display. The Waveform μP updates each section of Display Memory at the proper time, based on internal routines stored in Waveform Processor ROM and timing supplied by the Secondary Clocks via the Waveform Processor Clock and Bus Grant Decoding circuit. The Waveform μP also writes attribute changes (such as changes in horizontal position) to the Display Memory (when assigned the task by the System μP).

The Waveform μP addresses (in parallel) both the Waveform Save Memory and the Display RAMs via the Address Multiplexer (diagram 17). The System μP gates the address through to the Display Memory (the Vertical, Horizontal, and Attribute RAMs on diagram 16) via the Display Control Register (diagram 17). The Waveform μP then clocks the data out of its memory into the appropriate Display RAM.

Data Transfer to Display DACs

When the System μP initiates the display of the data stored in Display Memory, it writes (via its data bus) the starting address of that data to the Display Counter (diagram 17). It also outputs an address that latches, via the Register Select Circuit, the starting address into the Display Counter. Simultaneously, data from the System μP initiates, via the Display Control Register (diagram 17), a strobe to the Display State Machine. The Display State Machine then signals the Address Multiplexer, gating the address(es) output by the Display Counter through to Display Memory (diagram 16), and begins to gate a clock from the Display Clocks circuit to the Display Counter. The Display Counter increments for each (display) clock cycle, accessing successive addresses in Display Memory as the System μP clocks the data out of Display Memory.

The System μP uses data writes to the Mode-Control Register (diagram 17) to select which portion of the Display Memory (Vertical, Horizontal, or Attribute) or which register (Volts Cursors or Time Cursors) is selected for output to the Vertical or Horizontal DACs. The System μP also uses the Mode-Control Register to select, via the Horizontal Data Buffers, whether the waveform data in the Horizontal Ram is applied to the Horizontal or Vertical DAC, allowing either YT or XY displays.

It should be noted that the incrementing addresses supplied via the address latch are also applied to the Ramp Buffer. Since each incremental address corresponds directly to the data byte it addresses, and since the output of the Ramp Buffer (diagram 16) will be converted to a staircase waveform by the Horizontal DAC, the addresses can provide the horizontal deflection (or "ramp") necessary for YT displays.

Data Display

Data, waveform or other, is converted to two complementary output currents by each Display DAC. These currents are analog in nature, but reflect the ±256-bit resolution of the DACs. Therefore, the current outputs are a series of discrete analog levels (or steps, if the current is varying), each level corresponding to the 8-bit byte applied to the DAC.

The differential current outputs from the Horizontal and Vertical DACs are converted to single-ended voltages at the input to the Display Output circuitry. Those voltages then drive either the corresponding Horizontal and Vertical Vector Generators (diagram 18) for vector displays or the Horizontal and Vertical Output Amplifiers directly for dot displays.

The Vector Generators consist of a High-Current Difference Amplifier, a Sample-and-Hold circuit, and a Integrator to produce the vectors that connect the sample points in the display. Signals for vectored displays are continuously sampled and held, and integrated. The input voltage integrated is the difference between the voltage level of the sample presently being held and the intergrated level of the sample immediately preceding it. This action allows a smooth transition between the individual steps for a continuous display.

A Display Mode Switcher selects between the Vector Generator signals, a dots-only signal or an envelope display signal. With Envelope mode selected, the signal is passed through an rc integrator that produces vectors between the min-max data points of the Envelope Mode display.

The System μP, based on Front Panel settings, selects the display mode for the Vertical and Horizontal Vector Generators. The selected input, either Vector, Dot, Envelope, or Readout inputs, from each Vector Generator is coupled through to its corresponding Vertical or Horizontal Output circuit (diagram 18). There they are amplified and converted from single-ended to double-ended, to drive the Vertical or Horizontal plates of the crt (diagram 19). Both Vertical and Horizontal Output circuits have voltage offset and gain adjustments and are compensated for "spot wobble" (variations in beam placement on the crt screen with variations in beam intensity) by the Intensity circuit (diagram 6) via the Spot-Wobble Correction circuit.

DETAILED CIRCUIT DESCRIPTION

SYSTEM PROCESSOR

The System Processor (diagram 1) is the control center of all operations in the scope. It consists of an 8-bit microprocessor (μP), an 8-bit data bus, a 16-bit address bus, a prioritizing interrupt system, hardware address decoding, nonvolatile RAM space, and 272K bytes of bank-switched ROM.

The System Processor circuitry also coordinates the functions of the two other microprocessors in the 2430, the Waveform Processor and the Front Panel Processor.

System μP

System μP U640 executes instructions stored in the System ROM in order to initiate and control the various functions of this scope. Internally, the microprocessor has 16-bit data paths; externally it has an 8-bit data bus for communication and a separate 16-bit address bus. No address/data bus demultiplexing is necessary. The μP is driven by an external 8-MHz clock that is divided by four internally for a 2-MHz cycle rate. The number of cycles per instruction varies from a minimum of 2 to a maximum of 20, with the average being about 4 cycles per instruction. The μP executes, on the average, 1/2 MIP (Million Instructions Per second).

System μP U640 generates three signals used to control the communication activities of external circuitry. Of these signals, E and Q are for timing purposes. The rising edge of Q signals that the address on the bus is valid; data to the μP is latched on the falling edge of E. The third signal generated is the R/W signal. It is valid the same time the address is valid, and its state (LO or HI) determines whether an addressed device is written to or read from.

The E signal (U640 pin 34) and the Q signal (U640 pin 35) are ORed together by U840D to generate the HVMA (Host Valid Memory Address) signal. When HVMA at U840D pin 11 is HI, the address on the bus is valid. Once the external circuitry receives a valid address signal, it proceeds with the specified memory access. The signals used to enable and time these accesses are $\overline{RD}$ (read) and $\overline{WR}$ (write).

The $\overline{RD}$ signal is derived from U844A, which NANDs the HVMA signal with the μP R/$\overline{W}$ signal. Inverting buffer U572C provides added driving power to the R/$\overline{W}$ signal, and inverting buffer U884B reinverts it back to its original polarity before it is applied to NAND-gate U844A. The output of U844A is the $\overline{RD}$ signal, whose falling edge indicates the start of a read cycle. The rising edge of $\overline{RD}$ is coincident with the latching of the data read into μP U640.

The $\overline{WR}$ signal is derived from an inverted version of the μP R/$\overline{W}$ signal (via U572C) with a buffered μP Q signal (via U880D) NANDed by U844B. The output of this NAND-gate is a signal with a falling edge that indicates the start of a write cycle to the addressed device and a rising edge that latches data from the μP into the addressed device. The Q signal is used here instead of HVMA (as was used to generate $\overline{RD}$ to produce a data hold time of more than 100 ns as needed by the oscilloscope Time Base Controller circuitry.

Data Bus Buffer

Data Bus Buffer U650 provides buffering of the data bus lines. It is bidirectional to enable two-way communication between the System μP and the data bus. In normal operation, jumper J126 will connect the chip-enable pin to ground, and the buffer is enabled to transfer data. The direction of the transfer is controlled by the R/$\overline{W}$ signal from the System μP via inverting buffer U572C.

Moving test jumper J126 to its "KERNEL" position disables buffer U650 and forces it to its tri-state (high-impedance output) mode. The pull-up and pull-down resistors on the data bus lines, R742, R746, and R744, place an instruction byte on the μP data bus that causes the μP to repeatedly increment the addresses placed on its address bus lines through their entire range. This procedure is a troubleshooting aid that exercises a good portion of the address-decoding and chip-select circuitry.

Address Buffers

Address Buffers U632 and U730 provide buffering of the System μP address lines to the various addressable devices. The buffer chips are permanently enabled and provide both current buffering and electrical isolation for the address lines. Test point TP840 is provided as a source of an oscilloscope trigger signal when checking the

incrementing address lines in the forced "KERNEL" troubleshooting mode described in the "Data Bus Buffer" description.

System ROM

The System ROM (read-only memory) stores the commands and data used by System μP U640 to execute its control functions. The System ROM is made up of one 16K byte $\times$ 8-bit memory device, U670, that contains the System μP operating system, and four page-switched, 64K byte $\times$ 8-bit memory devices, U680, U682, U690, and U692 used for storage of all the additional operating routines. This gives a total of 272K bytes of ROM space. Each ROM is individually enabled by the ROM Select circuitry, and the addressed data will only appear on the system data bus when the $\overline{RD}$ (read) signal goes LO. Since μP U640 has the capability to address only 64K locations and has to address other things besides ROM, the System ROM is split into 17 pages. Address decoders U890A, U890B, and part of PC Register U860, select the page of ROM to be read from to allow the System μP to access the entire 272K byte ROM space.

Immediately after the power-up reset ends, μP U640 automatically tries to fetch the reset vector (the location of the first program instruction) from locations FFFE(hex) and FFFF(hex) in its address space. Anytime the System μP tries to access memory, the HVMA (host valid memory address) signal from U840D will be HI during the time the address is guaranteed to be valid. Addresses FFFE and FFFF have bits AE and AF (the two MSBs of the address bus) set HI; therefore, with the HVMA signal HI, NAND-gate U870D outputs a LO that enables U890A, and a $\overline{ROM1}$ select output is obtained from U890A for both addresses. The $\overline{ROM1}$ applied to the chip-enable input of ROM U670, along with the LO $\overline{RD}$ applied to its output enable, outputs the two 8-bit data bytes from location FFFE and location FFFF onto the system data bus via bus transceiver U660. The address contained in these bytes directs the μP to the start of its program, and the program is started.

When the μP needs information from one of the other System ROMs, it writes four bits of select data into register U860. Of these bits, PAGE-BIT0 and PAGE-BIT1, applied to 1-of-4 Decoder U890B, select which ROM chip of ROM0 is enabled. PAGE-BIT2 and PAGE-BIT3 are the most significant bits of the ROM addresses and determine which page of the enabled ROM is addressed.

Power-Up Reset

The Power-Up Reset circuit holds the System μP U640 reset for 100 ms after instrument power up to make sure that all instrument power supplies are operating properly. This delay ensures that the System μP begins the operating program with all electrical components in valid (defined) states after the instrument is powered on.

The Power-Up Reset circuit consists of a Texas Instruments® TL7705 Reset Controller U942 and some RC timing components. When the instrument is first powered up, the Reset Controller's $\overline{RESET}$ output is LO, holding the System μP reset at pin 37. The Reset Controller then monitors the power supply voltage at its SENSE input at pin 7. When the supply voltage at this input reaches operating tolerance, the Reset controller allows an internal current source to begin charging C938 at pin 3. After at least 100 ms (time is determined by the 10μf capacitor C938 and the 200K resistor R936), the voltage on C938 triggers an internal comparator in the Reset Controller and the Reset Controller removes the reset at pin 37 of the System μP by switching $\overline{RESET}$ HI.

The Power-Up Reset continues to monitor the power supply voltage at its SENSE input. This voltage is divided by an internal voltage divider and continuously compared against an internal voltage reference. If the power supply drops below operating limits for some reason, the Reset Controller drives $\overline{RESET}$ LO to reset the System μP, and, at the same time, it discharges C938. The normal power-up sequence previously described can then occur when/if the power supply comes back within limits.

In a normal power-down sequence, the System μP is notified in advance that power is going down via the non-maskable interrupt PWRUP from the Power Up circuit (diagram 23). The power supply remains up for a minimum of 10 ms after PWRUP is issued, and the System μP uses the time to calculate and save calibration constants, front-panel settings, and other information needed when it is repowered up. Once these "housekeeping chores" are completed, the System μP sets the PWRDOWN bit HI at pin 15 of U760, which pulls the RESIN (reset in) input of the Reset Controller LO through inverter U254E. This forces the Reset Controller to reset the System μP as previously discussed.

NOTE

If, for some reason, the System μP does not set PWRDOWN to trigger the reset, the Reset Controller does so when the power monitored at the SENSE input falls below operating limits (see previous discussion).

Interrupt Logic

The Interrupt Logic circuit provides a means by which other sub-systems may interrupt the normal program execution being done by the μP to request service. Three levels of interrupts are available in μP U640. The $\overline{NMI}$ (non-maskable interrupt) that occurs at power-down has priority over the other two interrupt levels. If either of the other

interrupts is present at the same time as the $\overline{NMI}$, the μP gives preference to the $\overline{NMI}$ and immediately branches to the power-down routine. The power-down routine performs the operations necessary for an orderly shut-down of the scope. A cyclical-redundancy checksum of the data stored in Nonvolatile RAM is calculated and stored back into that RAM. On power-up, that checksum is used to verify the validity of the parameters and settings stored in the Nonvolatile RAM. To prevent a possible 50-ohm overload of the Channel 1 or Channel 2 input circuitry during times that the instrument is off, part of the power-down routine is to make certain that input coupling is set to a high-impedance state.

The next interrupt in priority after the $\overline{NMI}$ is the $\overline{FIRQ}$ (fast-interrupt request). It is produced by flip-flop U894A in response to a 2 ms clock signal from the Time Base circuit (diagram 8). The 2 ms clock sets the $\overline{FIRQ}$ line LO every 2 ms to signal μP U640 that it is time to do the time-critical tasks like updating the DAC System. When the fast-interrupt request has been serviced, the μP clears the $\overline{FIRQ}$ latched into U894A by outputting address 6012h. This address is decoded by 1-of-8 Decoder U884 to generate a $\overline{CLRFIRQ}$ (clear fast-interrupt request) signal that resets flip-flop U894A. Servicing of a fast-interrupt request differs from other interrupt requests in that the contents of only two μP registers are pushed to an internal stack (instead of all the μP registers), allowing the μP to respond faster.

The lowest priority is given to the combined signal forming the $\overline{IRQ}$ (interrupt request). This interrupt allows various sub-systems to get attention from the System μP. NOR-gate U850B outputs a LO when any of the five conditions occur. Inputs to NOR-gate U850B are from: the GPIB (General Purpose Interface Bus), the Display circuitry, the Front Panel, the Waveform μP, and the Trigger System. Of these, the latter three interrupts may be masked off (disabled) by the μP by writing LO mask bits into register U760 which are then applied to AND-gates U880A, U880B, and U880C. A LO input to one input of an AND-gate holds the associated output pin LO and prevents an interrupt signal from being gated through to NOR-gate U850B. The Waveform μP may mask the Display System interrupt (DISDN) from the System μP by placing a LO on pin 5 (MDISDN) of AND-gate U580B from register U550 (diagram 2). The Waveform μP thereby can gain first access to the Display System if it needs to do display updates before the System μP sees that the Display System is finished with its last task. When the Waveform μP is done, it writes the MDISDN interrupt HI to let the System μP know that it is finished with the Display System and the Display System is ready to be restarted.

When an $\overline{IRQ}$ interrupt is detected, the μP executes a read of location 6010h which is the address of Interrupt Register U654 (an octal buffer). That address is decoded by 1-of-8 Decoder U884 to set $\overline{INTREG}$ LO and enable U654. The enabled buffer passes the status of the various interrupt lines at its inputs to the data bus for the μP to read. From the status bits read, the μP determines which circuit caused the interrupt and branches to the called for interrupt service routine. If more than one interrupt is pending, the System μP IRQ interrupt handling routine decides which one needs to be (or can be) handled first. The order in which it handles these interrupts depends on the current activity of the System μP.

Besides interrupt status, three other status bits are read from the Interrupt Register. These are the DCOK (dc ok) signal from the power supply (check during the calibration routine register checks), BUSGRANT from the Waveform μP, and $\overline{FPDNRD}$. DCOK signifies that the various power supply voltages are within proper limits; BUSGRANT indicates that the Waveform μP has relinquished bus control in its operating space and that those addresses are now mapped into the System μP address space. $\overline{FPDNRD}$ indicates that the Front Panel μP has read the data sent to it from the System μP.

System Address Decode Circuit

The System Address Decode circuit uses several of the system address bits, along with other control signals, to connect the System Data Bus (via the Memory Buffer) to System RAM and ROM (called System Memory, collectively) for those addresses that map to those memories. It also isolates the System Data Bus from System Memory when the System μP output addresses that map to other memory devices or certain input/output registers. Some control signals are routed from this decode circuit to other circuits and are used to decode enables for those circuits.

MEMORY BUFFER. U660, a bi-directional buffer, connects or isolates the System Data Bus from System Memory depending on whether enabled or disabled by the output of AND-gate U580A. Direction of data transfer is controlled by $\overline{WR}$ (write) line from the system processor. When devices other than System ROM or System RAM are addressed, the buffer outputs are switched to a high-impedance state to isolate the memory devices from the data bus.

MEMORY MAP. Figure 3-2 is a memory map showing the different memory areas and the address blocks they occupy on the System Processor and the Waveform Processor Data Bus. Addresses output by the System Processor and/or the Waveform Processor access the memory indicated in the address block depending on how those addresses are decoded. Refer to Figure 3-2 as the address blocks are discussed (both here and later for the Waveform RAM).

As indicated by the memory map, addresses from 0000h-7FFFh are overlapping addresses; that is, if they are originated by the System Processor, they may map to (access) memory locations or registers connected to either

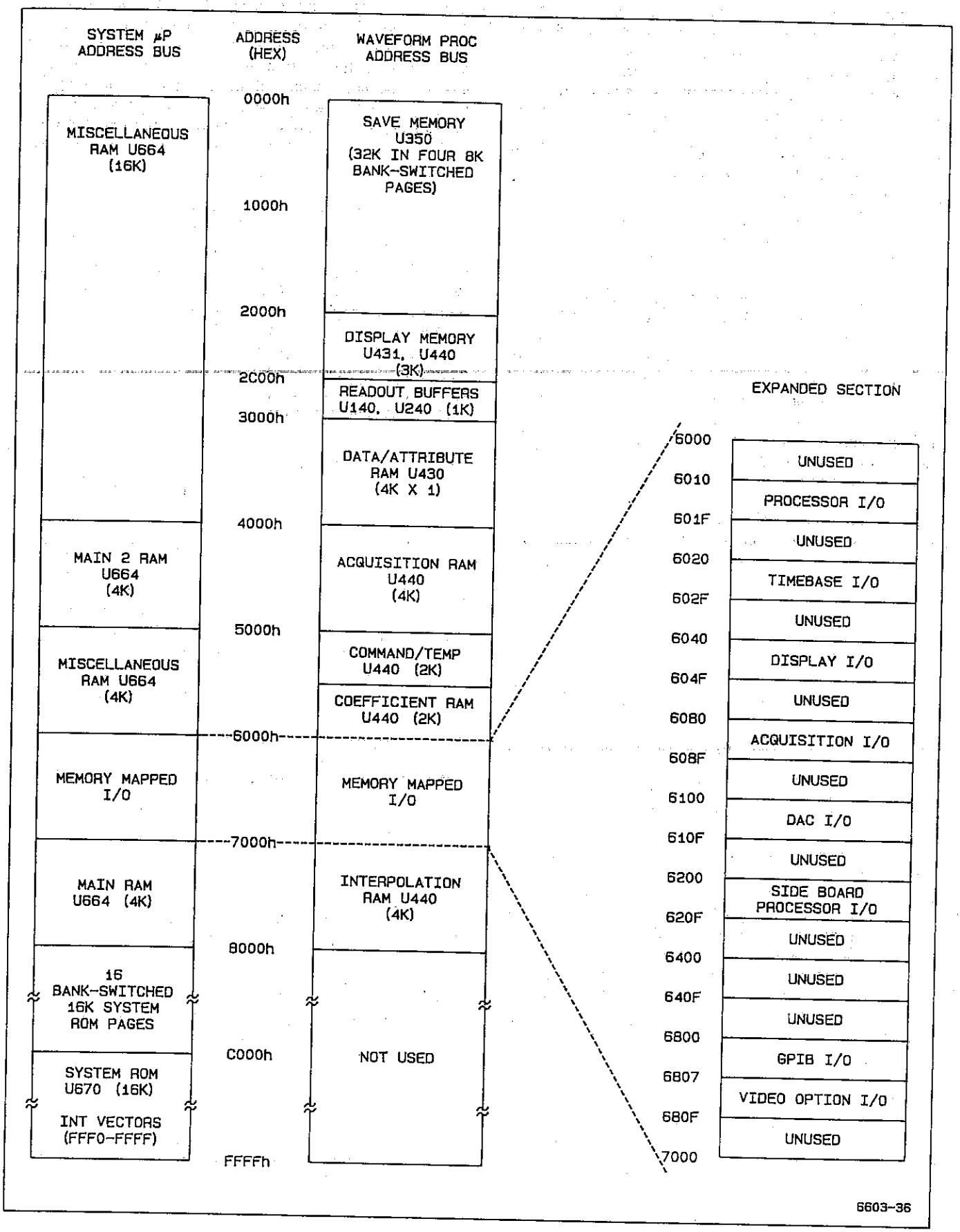


Figure 3-2. Simplified Memory Map

the System Data Bus or the Waveform Processor Data bus. If they are originated by the Waveform Processor, they access the memories indicated on the Waveform Processor Bus. The following description of the address decoding is for System Processor addresses and how the System Address Circuit outputs control signals to the Memory Buffer and to the address decoding circuit for the Waveform Processor (diagram 2). For information on how the Waveform Processor's address decoding circuitry uses these signals, see "Waveform Processor Operation" in this section.

ADDRESSES 8000h-FFFFh. All addresses from 8000h-FFFFh have AF set HI. This HI is AF is inverted (via U866C) and routed to U580A. With the inverted AF bit holding the input of AND-gate U580A LO, the output of the gate holds the Memory Buffer U660 enabled (LO). As shown in the memory map, all addresses in this range are System ROM accesses and require System Data Bus connection to the System Memory Data Bus. Locations 8000h-FFFFh are not used to address any other memory devices outside System memory (decoding for the paged System ROM was discussed under "System ROM" in this section).

ADDRESSES 0000h-7FFFh. All addresses in this range have the AF bit set LO. With AF LO, the inverted AF signal holds a HI at one input to the dual-input AND-gate U580A. The output of this AND-gate (and the enabling of U660) is then controlled by the output of OR-gate U332A.

When the System Processor wants these address ranges to map to the Waveform Processor Data Bus (i. e., wants the System Data Bus and the Waveform Data Bus connected) , it either asserts BUSREQ to the Waveform μP to receive BUSGRANT, or it asserts BUSTAKE to force BUSGRANT. BUSGRANT at the input of OR-GATE U250D forces a HI to the input of AND-gate U862B. If this is not a $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$ memory access, $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ from 1-of-8 Decoder U668 are both HI and U862B output is driven HI by the BUSGRANT. This HI is coupled through U332A and U580A to disable the U660 Memory Buffer and disconnect the System Data Bus from System Memory. $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ are routed to decoding circuitry and used to connect the System Data Bus to the Waveform Data Bus (see "System μP Access" under "Waveform Processor Operation" in this section).

If either of the host RAM enables $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$ are LO, the 1-of-8 decoder U668 has decoded address lines AC, AD, and AE to determine that the addresses range from 4000h-4FFFh or from 7000h-7FFFh. In these address ranges, the LO host RAM enable holds off the BUSGRANT-forced HI at the output of U250D from driving the output of AND-gate U862B HI. If the System Processor is accessing these locations in Waveform Processor RAM, it asserts WPRAM HI (Waveform RAM) at the input to OR-gate U332A. This HI is coupled through U332A and AND-gate U580 to disable U660 regardless of BUSGRANT, $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$. BUSGRANT and WPRAM are routed to decoding circuitry to connect the System DATA Bus to the Waveform Data Bus.

If the System Processor is NOT accessing Waveform Processor RAM for the 4000h-4FFFh or 7000h-7FFFh address space, WPRAM is disabled LO. With either $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$ enabled LO, the output of U862B is driven LO. This LO lets OR-gate U332A, and then AND-gate U580A, switch LO and enables Memory Buffer U660 to connect the System Data Bus to the System Memory Bus. The $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ memories are then accessed.

If the System Processor is NOT accessing Waveform Processor RAM or a MAIN-section of System RAM, BUSGRANT and WPRAM are NOT asserted HI and $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ are not asserted LO. In this case, the output of four-input AND-gate U862A controls the enabling/disabling of the Memory Buffer. U862A combines with AND-gate U432B to form a five-input AND-gate function, with output Y0-Y3 and Y5 connected to the five inputs. If the address is in the range of 0000h-4FFFh or 5000h-5FFFh, 1-of-8 decoder U668 decodes a LO output to one of the five ANDed inputs. U862A outputs a LO which is ORed (by U250D) with the disabled BUSGRANT (LO) to hold off AND-gate U862B. The LO at the output of U862B is passed through U332A (WPRAM is LO) and U580A to enable the Memory Buffer and connect the System Data Bus to the System Memory. The LO output of U322A, $\overline{\text{CYSYS}}$, also enables the System RAM for this Miscellaneous RAM access.

ADDRESSES 6000h-6FFFh. Addresses in this range either access devices on the Waveform Processor bus or directly access devices on the System Data Bus. If the address is in this range, U668 decodes Y6, $\overline{\text{HMMIO}}$ LO.

Since Y6 is LO, all other outputs, including those driving the five inputs to AND-function U862A/U432B, are HI. With the five inputs to AND-function U862A/U432B all HI, its output is HI to U862. With the remaining two decoder outputs U862B, $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$, set HI, AND-gate U862B outputs a HI that holds the Memory Buffer disabled for ALL HMMIO accesses. $\overline{\text{HMMIO}}$ is inverted via U866B and is routed, along with address bits A3 and A4, to decoding circuitry (Diagram 2) to determine when the System Data Bus connects to the Waveform Data Bus for HMMIO accesses.

Host Memory-Mapped I/O

To permit the System μP to control the hardware functions of the scope, several control registers have been assigned to unique addresses within the μP address space (memory-mapped). These registers appear as blocks of read-only, write-only, or read-write memory to the System μP. The data bits handled by these registers control specific hardware functions, and the commands written will not violate any hardware restrictions.

As mentioned in "System Address Decode Circuit", the block of addresses from 6000h to 6FFFh corresponds to the host memory-mapped input/output ($\overline{\text{HMMIO}}$) block. Addresses within this block are decoded to produce a LO $\overline{\text{HMMIO}}$ signal to 1-of-8 Decoder U884 and Octal buffer U830. The three MSBs of the I/O address block and the HVMA (host valid memory address) are decoded by 1-of-8 decoder U668 to decode the I/O addresses between 6000h and 6FFFh.

One-of-eight Decoder U884 uses the $\overline{\text{HMMIO}}$ line and address bits A3 and A4 as enabling signals. Address lines A0 and A1 and the R/$\overline{\text{W}}$ line from the processor (via inverter U572C), select one of the eight outputs of U884 to go LO when the Decoder is enabled. Table 3-1 shows the registers accessed by this decoding.

Inverting buffer U830, enabled by $\overline{\text{HMMIO}}$ for I/O operations, applies the inverted middle bits of the address bus to various functional modules as selects. The firmware routines will allow only one of these select bits to be set LO at a time. In the selected circuit, further address decoding is enabled. Figure 3-2 illustrates the System μP address memory map and shows the blocks assigned for memory-mapped I/O. Each of the memory-mapped I/O blocks consists of 16 consecutive addresses from 6000h to 7000h with various functions assigned to specific addresses. These functions include clocks, chip enables, and circuit enables. Each is explained in the descriptions of the circuits they affect.

System RAM

The System RAM provides temporary storage of data used in execution of the various control functions of the System μP. In addition, long-term power-off storage of system-calibration constants and front-panel settings is provided, allowing the instrument to power on in the same state it was in when it was turned off.

The System RAM consists of a single memory device. It is nonvolatile RAM, that is, a battery-backup circuit is used to maintain data when power is off. The μP U640 controls the direction of data flow via the $\overline{\text{WR}}$ (write) and $\overline{\text{RD}}$ (read) control lines.

NOTE

Although all the data in this memory device is backed up and is, therefore, nonvolatile, that part of the System RAM reserved for data that NEEDS to be backed up (such as the calibration constants and front-panel settings) is referred to as NVRAM throughout this section. Parts of System RAM that do NOT NEED backing up are referred to as volatile RAM or just RAM.

Table 3-1
Host Memory-Mapped I/O

W/R	A1	A0	Output Signal
LO	LO	LO	INTREG (read Interrupt Register)
LO	LO	HI	PMISCIN (Processor miscellaneous inputs)
LO	HI	LO	CLRFIRQ (clears FIRQ flip-flop)[a]
LO	HI	HI	NC
HI	LO	LO	PCREG (write Processsor Control Register)
HI	LO	HI	PMISCOUT (write Misc Register)
HI	HI	LO	TVREG (write Video Option Register)
HI	HI	HI	WDREG (write Word Probe and GPIB LED Register)

[a]**To clear the Fast-Interrupt Request, the μP does a read of the assigned address even through an actual register does not exist. The decoded output performs the reset function and no data is transferred.**

The chip-select circuit for System RAM U664 consists of Q842, Q960, CR944, and associated components. With instrument power off, no bias current for Q960 is available, and the transistor is off. Power for maintaining the stored contents of the RAM is applied to U664 from the Battery circuit; with Q960 off, the chip enable input of U664 is also pulled HI via R764 to switch the I/O pins to their high-impedance state. This is the "low-power standby mode," and the contents of U664 are maintained as long as the Vb_{cc} supply and CE (chip enable) pins are held above +2 volts.

When instrument power is applied, a switching circuit in the Battery stage supplies power for the RAM, and the normal power supplies provide bias currents for the chip-select string between U332A and U664. As the power supplies are coming up, operations on the address bus are undefined, which could cause U332A to try to enable U664. To prevent this, the $\overline{\text{RESET}}$ signal from the Power-Up Reset stage is applied to the base circuit of Q960 through diode CR944. This LO keeps the transistor biased off until the power-up $\overline{\text{RESET}}$ signal returns HI; at which time the data on the address bus is stable.

With normal power on, when OR-gate U332A decodes a System RAM access, its output goes LO to turn off Q842. R956 then pulls up on the base of Q960, turning that transistor on and pulling the chip-enable pin of U664 LO to enable the System RAM. The RAM enable is removed when the output of U332A goes HI, turning Q842 back on and robbing the base current from Q960. With Q960 off, R764 pulls the chip-enable input of U664 HI to disable the RAM.

Miscellaneous Registers

The Miscellaneous Registers allow the System μP to initiate and control various processes by writing control words to two address-decoded locations. The Miscellaneous Registers also contain an address-decoded buffer used to read certain bits of instrument status.

The $\overline{\text{RESET}}$ line holds all of the outputs of Processor Control Register U860 LO until the Power-Up Reset goes HI, ensuring that the functions controlled by the PC register outputs start in known states. To load U860 the System μP writes data to location 6014h, generating an address-decoded $\overline{\text{PCREG}}$ clock. This rising edge of the $\overline{\text{PCREG}}$ clock when the clock returns HI causes the data on the data bus to be written into the register. Table 3-2 illustrates the select functions of the PC Register output bits.

Operation of U760, the Processor Miscellaneous Register (PMREG), is similar to U860 just described. Data is written into the register with the $\overline{\text{PMISCOUT}}$ (processor miscellaneous outputs) clock when address 6015h is decoded by U884. Table 3-3 explains register functions.

Table 3-2
Processor Control Register Functions

Bit	Output Name	Output Function
0 1	PAGE-BIT0 PAGE-BIT1	ROM enable selection signals for Bank-Switched System ROM.
2 3	PAGE-BIT2 PAGE-BIT3	Select a page in Bank-Switched System ROM.
4	WPRESET	Resets Waveform μP.
5	WPKERNEL	Places the Waveform μP in "Kernel" mode for diagnostics.
6	BUSREQ	System μP requests to take control of the Waveform μP busses.
7	BUSTAKE	System μP takes control of the Waveform μP address and data busses.
8	DIAGO	Diagnostic bit 0—verifies that data can be written to the PC register.

The Processor Miscellaneous buffer (PMBUF), U854, at address 6011h, allows the System μP to monitor the activities of various other circuits. By reading the data byte from location 6011h, the System μP can check for the presence of a Word-Trigger probe and for Waveform μP and Front Panel μP interrupts. For diagnostic routines and self-check, correct operation of registers U760, U860, and U754 is verified by writing known values to the diagnostic bits (DIAG0, DIAG1, and DIAG2) then reading them back. If both HI'S and LO'S can be written to and read from these diagnostic locations, fairly high confidence may be placed in the addressing and selection of the registers and their data paths.

Battery

The Battery circuit supplies standby power to the System RAM that allows instrument calibration constants and front-panel settings to remain stored for long periods of time (greater than three years) when instrument power is turned off. A switching circuit turns off the battery (BT800) current source while normal instrument power is applied. A battery monitor circuit warns the Front Panel μP (and thereby the user) of a low-voltage condition (indicating that

Table 3-3
Processor Miscellaneous Register (PMREG) Output Functions

Bit	Output Name	Output Functionss
0	MWPDN	Masks off (disables) Waveform Processor Done interrupt.
1	MSYNTRIG	Masks off Synchronous Trigger interrupt.
2	MFPINT	Masks off Front-Panel interrupt.
3	STEP COMP	Indicates the AutoStep Sequencer has completed a sequence step.
4	SEQOUT	Indicates the AutoStep Sequencer has completed a sequence.
6	BELL	Indicates an event occurred which normally rings instrument's internal warning bell.

it is time to change the battery) or an over-voltage condition (indicating that reverse current is attempting to charge the lithium battery).

With normal instrument power applied, transistor Q806 will be turned on by the base-bias voltage-divider circuit formed by R812 and R815. Base current is then supplied through Q806 and R800 to turn on Q804. This is the normal operating mode, and operating current for Nonvolatile RAM U664 is supplied via Q804 from the $+5\ V_D$ supply. During normal operation, capacitor C904 is held charged through CR902 but isolated from the RAM power source by reverse-biased diode CR900.

With instrument power turned off, transistors Q806 and Q804 are both turned off. The positive charge potential stored by capacitor C904 forward biases CR900 and pulls the chip-enable pin of U664 HI through R764. This disables RAM U664 and switches its I/O ports to high-impedance states. Operation in this state is the "standby" mode in which data in U664 is maintained using minimal supply current.

The eventual charge loss from capacitor C904 causes its output voltage to drop below that of Backup Battery BT800 (a lithium battery), and diode CR900 again becomes reverse biased. The standby current for U664 is then supplied from the battery via CR802 (and R900 in the return path). Diode CR802 acts as the current switch and prevents reverse current through the lithium battery during normal power-on operation. Resistor R900 provides reverse-current limiting in the event that CR802 becomes shorted.

BATTERY WARNING CIRCUIT. Operational amplifier U940A is a very high impedance buffer to limit current drain of the battery. Its buffered output voltage is applied to the Front Panel μP (diagram 3) to monitor for both low-voltage and over-voltage conditions of the lithium backup battery. A battery-error condition found at power-on or with the Extended Diagnostics will cause the BATT-STATUS test to fail. That test may then be selected to run at the next lower level in the test hierarchy to determine if the battery is undervoltage or overvoltage. The warning circuit is operational only when normal instrument power is applied. Resistor R802 provides additional circuit impedance that prevents any appreciable discharging of the battery by the voltage-sensing circuit.

WAVEFORM PROCESSOR SYSTEM

The Waveform Processor System (diagram 2) performs the high-speed data-handling operations needed to produce and update displays of acquired data points on the crt including averaging, enveloping, adding, multiplying, and interpolation of the waveform data. It accepts task information from the System μP and then carries out the assigned tasks without further need of the System μP. When that task list has been completed, it sends an interrupt to the System μP to inform it that another list of tasks can be accepted.

The Waveform μP memory space is accessible by the System μP, allowing the System μP to send commands to the Waveform μP and to read any desired result or data location especially for the GPIB I/O functions.

Waveform μP

Waveform μP U470 is a specially designed, high-speed microprocessor with a 16-bit multiplexed data and address bus and separate 12-bit instruction-address and 16-bit instruction-data busses. The Waveform μP is clocked at 2.5 MHz and executes one instruction each clock cycle. Internally the Waveform μP uses a 32-bit wide instruction word. Therefore, to enable it to obtain a complete instruction for execution with each μP cycle, instructions are "double-prefetched." Two 16-bit halves of the instruction are fetched from the instruction bus with each cycle at a 5 MHz rate, so that the instruction words are 32 bits wide.

Initially, with power-on, $\overline{\text{WPRESET}}$ (Waveform μP reset) from Processor Controlled Register U860 (diagram 1) will be LO, holding the processor reset via U270C. This reset remains in effect until the System μP writes a HI bit to the $\overline{\text{WPRESET}}$ output of U860 to remove the reset and enable the Waveform μP. The System μP also holds the Waveform μP reset while it is updating the command list in RAM of the next task that the Waveform μP is to perform. This reset occurs at the completion of each set of tasks given to the Waveform μP and is released when the new task list is in place in the Waveform μP Command RAM, U440.

Upon release of $\overline{\text{WPRESET}}$, the Waveform μP fetches the first two 16-bit words from its instruction ROMs, U480 and U490, at a 5 MHz rate and forms them into a 32-bit instruction word. Waveform μP U470 then executes the first instruction and at the same time it "prefetches" the next 32-bit word from the instruction ROM (the next instruction). The Waveform μP continues fetching instructions to carry out its internal initialization routine until that is completed, and it then looks in Command RAM at a vectored location to find the first task in the task list.

The first instruction in the task list tells the Waveform μP what is to be done. The μP then switches to the routine in ROM to get the instructions that do that job. Part of that routine might be to get the arguments for the task. When the arguments are in place, the Waveform μP then finishes the task routine. When done with the first task, the Waveform μP looks at the task list for the next task. It keeps doing the commands and arguments for each task until the entire task list is done. The last task of every task list is the WPDN task (Waveform Processor Done). Upon receiving that task, the Waveform μP sets the WPDN bit to the System μP Interrupt circuit HI, informing the System μP that it is finished. It then enters a "loop forever" state to wait for its next set of instructions. When the System μP checks the interrupt register and finds WPDN HI, it resets the Waveform μP and writes a new list of tasks to the Waveform μP Command RAM.

WAVEFORM μP OPERATION. When the Waveform μP gains control of the waveform bus, it sequentially moves the 1024 data points for each channel (512 min/max pairs in envelope) from the Acquisition Memory (diagram 8) to the Save Memory (U350). When the Waveform μP does a display update, it selects the required data points needed for each waveform display requested (according to the mode selected) from Save Memory and moves them to the Display Memory (diagram 16). At the end of the display update, DISDN (display done) from the Display Control (diagram 17) goes HI to interrupt the Waveform μP (and the System μP if the Waveform μP is also done and permits the signal to be gated to the System μP via AND-gate U580B, diagram 1). This tells the Waveform μP that the current display cycle has completed and the next update to Display Memory may be started.

When in ENVELOPE acquisition mode with more than a one acquisition accumulation to be displayed, the data bytes stored in Save Memory are not automatically overwritten with each acquisition. As the data bytes are being transferred from Acquisition Memory to Save Memory, they are compared by the Waveform μP. If the new data byte does not exceed the current maximum or minimum value in Save Memory location that it is being compared with, that Save Memory location is not overwritten (until the envelope acquisition is reset to start a new accumulation).

In AVG acquisition mode, data from the Acquisition Memory is averaged with the waveform data in the Save Memory, and the Save Memory is then rewritten with the averaged waveform data. Waveform adds, multiplies, expansions, and interpolations are performed by the Waveform μP on the Save Memory data prior to transfer to the Display Memory for display.

WAVEFORM μP ADDRESS ENABLING. The 2.5 MHz System Clock signal CLK1 from the Clock Divider U710 (diagram 7) is inverted by U866E and ORed with the skewed 2.5 MHz CLK3 signal by OR-gate U264B. The timing of this ORed signal is such that the output of U264B goes HI when the address on the input pins of Waveform Address Registers U562 and U364 is guaranteed to be valid. Inverter U270B inverts the output from the OR-gate (WVMA—waveform valid-memory address), and when that output again goes LO, the rising edge of the inverted WVMA signal on the clock input of the Waveform Address Registers latches the 16-bit address from the Waveform μP into the registers.

ADDRESS LATCH. U366, a dual 4-to-1 multiplexer, and Address Latches U364 and U562 couple a modified version of the 16-bit address output by the Waveform μP (DAD0-DADF) to the Waveform Processor Address Bus (WA0-WAF). Addresses latched to the Waveform Processor Address Bus remain on that bus for the entire Waveform μP cycle.

Due to its architecture, the Waveform μP outputs different address blocks than those required to access the various memories on the Waveform Processor Data Bus (see Figure 3-2). U366 selects either address bit DADC or DADB for output to address WAB of the Waveform Processor Data Bus, depending on the condition of its three most-significant address bits, DADC, DADE, and DADF. AND-gate U276B detects when these bits are all HI and outputs a HI to the "A" select input of the multiplexer.

With the "B" select input held HI for all Waveform μP accesses by $\overline{\text{BUSCONNECT}}$, U366 routes DADB to address bit WB via address latch U562.

If any of the three most-significant Waveform μP address bits are low, DADC is coupled to address bit WB. This action translates the addresses output by the Waveform μP to those required on the Waveform Processor Bus.

If $\overline{\text{BUSCONNECT}}$ is LO, the access is a System Processor access and BUSGRANT is HI. BUSGRANT disables the Address Latches and the decoding action of U366 does not affect the address on the Waveform Processor Bus. BUSGRANT is inverted via U254B enables the Bus Connect Address Buffers to connect the System Address Bus to the Waveform Processor Bus.

Test point TP562 on address line WAA provides a trigger source for an external test oscilloscope when examining address waveforms in the Waveform μP "KERNEL" mode. As the KERNEL mode exercises address lines WA0-WAA, WAA is used as the trigger point.

WAVEFORM μP READ/WRITE ENABLING. Once latched, the address is removed from the bus and, depending on whether μP U470 is supposed to be reading or writing, data will be read into the processor from data bus buffers U360 and U560 or written to the WD (waveform data) bus via U360, a bidirectional data bus buffer. To read data into the processor, the HI R/$\overline{\text{W}}$ (read-write) signal is applied to NAND-gate U870C where it is NANDed with $\overline{\text{CLK1}}$. During the half period that $\overline{\text{CLK1}}$ is HI (CLK1 is LO), the gated output from U870C is the $\overline{\text{WRD}}$ (waveform processor read) in its LO (asserted) state. The LO is applied to the direction-enabling input of bidirectional buffer U360 via U542B. This LO enables U360 for a read from the WD (waveform data) bus, and the addressed 8-bit word on the WD bus is applied to the center eight lines of the processor 16-bit address/data bus.

The four least significant bits (LSB) and the four most significant bits (MSB) of the data applied to the WD bus come from buffer U560, which is enabled via U250B and U250A for processor reads. The four LSBs are always LO (guard bits), while the four MSBs will be set to the same level as the WD7 bit (sign-extended) of the center eight bits. This placement of the 8-bit data in the center of the 16-bit bus provides a reasonable tradeoff between dynamic range (12 bits) and guard bits (4 bits).

To write data out of the Waveform μP to the WD bus, the $\overline{\text{WRD}}$ level applied to the direction-enabling pin of U360 will be HI. The center eight bits of the Waveform μP data bus will then be buffered onto the WD (waveform data) bus by U360 and written to the currently addressed location. During writes to the WD bus, the HI level of $\overline{\text{WRD}}$ disables buffer U560, via U250B and U250A, to isolate it from the Waveform μP address/data bus.

SYSTEM μP ACCESS. When the System μP needs to do an access in the Waveform μP address space, it checks its software copy of PCREG to see if the Waveform μP is reset. If it is not reset, the System μP asserts BUSREQ (bus request) to the Waveform μP and waits until the Waveform μP outputs a BUSACK (bus acknowledge) to OR-gate U332D. The output of U332D is the BUSGRANT signal that, when HI, disables the Waveform μP data buffers, address registers, and memory control lines.

When Waveform μP U470 is being held reset (inactive) and cannot possibly respond to a BUSREQ, the System μP instead asserts BUSTAKE to OR-gate U332D when it needs to take control of the Waveform μP address space. The System μP can also assert BUSTAKE during diagnostics in the event of a Waveform μP failure to release the bus after a BUSREQ is given.

With BUSGRANT asserted HI, the inverted BUSGRANT, $\overline{\text{BUSGRANT}}$ is output by inverter U254B and enables Bus Connect Address Buffers U262, U260, and U564. The enabled buffers connect the System μP address bus and control signal lines to their counterparts from the Waveform μP. The Bus Connect Data Buffer U552, a bidirectional device, is then enabled and directed by control signals from the System μP for data transfers to and from the Waveform μP data bus.

Decoding circuitry uses the signals WPRAM, $\overline{\text{MAIN}}$, $\overline{\text{MAIN2}}$, and HMMIO; System-Address bits A3, A4, and AF; and BUSTAKE/BUSGRANT to determine when to enable U552 and connect the System Data Bus to the Waveform Data Bus. The addresses that produce accesses to the Waveform RAM (and require U552 to be enabled) are shown as are noted on the memory map, Figure 3.2. (Also, see "System Address Decode", appearing earlier in this section.)

The Bus Connect Data Buffer is enabled when the output of the dual-input AND-gate U432D steps HI and the output of U254D steps LO. With BUSGRANT asserted HI, the output state of U850A depends on the state of its other input which is controlled by the output of OR-gate U850A. Any HI on U850A's inputs drives its output LO. This LO output holds the output of U432D LO and U552 disabled HI via U254D.

One input to U850A is $\overline{\text{BUSGRANT}}$. Since BUSGRANT is HI, $\overline{\text{BUSGRANT}}$ is LO a few nanoseconds after BUSGRANT enables. While HI, $\overline{\text{BUSGRANT}}$ holds U850A's output LO, preventing transients from enabling the Bus Connect Data Buffer. After the few nanoseconds $\overline{\text{BUSGRANT}}$ has no effect on decoder operation.

If the address-bit AF is HI at the input to NOR-gate U850A, the address on the System Address Bus is between 8000h-FFFFh. These addresses map only to System ROM; therefore, the access cannot be a Waveform Processor access. The HI AF-bit at the input to U850A holds its output LO and, via inverter U254D, the Bus Connect Data Buffer is disabled.

If either $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$ are LO, the System Processor is accessing the 4000h-4FFFh or 7000h-7FFFh address space, and WPRAM determines whether the access is to the Waveform RAM space. If WPRAM is disabled LO at the inputs to OR gates U840A and U840B, one of the outputs of those gates will be LO, depending on which signal, $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$, is also LO. The LO output will be inverted HI by either U254C or U254F, and the output of NOR-gate U850A will be LO. Again via inverter U254D, the Bus Connect Data Buffer is disabled.

If WPRAM is enabled HI, the outputs of both U840A and U840B are HI and are inverted LO by UU254F and U254C, respectively. Since this is not a System ROM (AF-bit) or a HMMIO access, the rest of the inputs of U850A will be LO and the output of U850A will go HI. The Bus Connect Data Buffer will be enabled by the LO at the output of inverter U254A.

If HMMIO is HI at the input to U874B, the access is for the 6000h-6FFFh address space. Whether or not the access connects the System Processor the Waveform Data Bus depends on System Address Bits A3 and A4.

For 6000h-6FFFh addresses in the eight upper ranges (6018h-601Fh, 6038h- 603Fh, etc.), both bits are HI; for the eight lower address ranges (6000h-6017h, 6020h-6037h, etc.), at least one of the bits will be LO. With one or both of the A3 and A4 bits LO at NAND-gate U874D, its output must be HI. This HI is coupled to one input of NAND-gate U874B (the other input of U874B is held HI by HMMIO) and its output is forced LO. This output is connected to the input of U874A, an inverter-configured NAND-gate, and holds the output of the device and the input to NOR-gate U850A HI. The Bus Connect Data Buffer is held disabled as previously described.

If both A3 and A4 are HI, NAND-gate U874D's output goes LO. This LO drives the output of NAND-gate U874B HI and the output of U874A LO. With the other inputs to U850A LO, its output goes HI and enables the Bus Connect Buffer via U254D. Waveform μP RAM

To summarize, the conditions that must be present for the decoding circuitry to produce an enable to the Bus Connect Data Buffer are:

1. $\overline{\text{BUSGRANT}}$ LO—Waveform μP has relinquished the busses;

2. $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ HI—This is not a "System RAM" Main Memory access;

3. Address bit AF is LO—This is not a "System ROM" access, and either:

   a. HMMIO is LO—The address is not a System μP memory-mapped I/O location, or

   b. It is a memory-mapped I/O location and address bits A3 and A4 are HI (the address is within the top eight I/O addresses ranges of the System μP).

Addresses residing in the System μP memory space should not access the Waveform μP memory space, and are thus excluded from access by U850A and the associated input logic gates. Addresses not excluded will cause a System μP access into the Waveform μP memory space.

Waveform μP ROM

The Waveform μP ROM consists of two 8K-X-8-bit ROM devices connected in parallel to form an 8K-X-16-bit storage memory for Waveform μP waveform data handling commands. The Waveform μP "double-fetches" data from this ROM space by reading in two 16-bit bytes of command data during each Waveform μP clock cycle. This method of reading the commands makes the Waveform μP command memory space look like a 4K-X-32-bit ROM. The 32-bit instruction word formed by the two fetches adequately defines any Waveform μP operation and allows the Waveform μP to execute one instruction for each 2.5 MHz clock cycle.

The chip-select pins of Waveform μP ROMs, U480 and U490, are both connected to a +5-V supply through R376. During normal operation, Waveform KERNEL jumper (P128) is installed, and the chip selects of both ROMs are shorted to ground and are constantly enabled.

The addresses of instructions to be read are determined by the 12 instruction-address bits output from the Waveform μP and by the state of the 5-MHz clock. The 12 address bits from U470 are the most significant address

bits for any given instruction. The 5-MHz clock applied to ROM address inputs A0 through delay line DL580 and associated components delays the least significant address bit enough delay to provide the needed data-hold time. The state of the 5-MHz clock will be LO to access the first 16 bits of an instruction word. The state of the A0 address line then goes HI, and the second half of the 32-bit instruction is obtained from the next higher memory location. This address selection scheme is the "double-fetch" of instruction data mentioned previously in the Waveform μP description.

Removing jumper P128 disables the Waveform ROMs and places their outputs into the high-impedance state. The pull-up and pull-down resistors within resistor packs R474 and R590 place a "NOP" (no-operation) instruction byte on the instruction bus. A NOP command causes the Waveform μP to increment through the first 12 bits of its address range on the 16-bit DAD bus and through all the addresses of its IA bus. This "KERNEL" mode allows the Waveform μP address bus and address decoding to be exercised for troubleshooting and diagnostic purposes.

Address Decode

The Address Decode circuit monitors the Waveform μP address bus to develop the appropriate enabling signals to the memory or I/O device that is to be accessed.

Block decoding is done by one-of-eight decoder U570, which uses address lines WAC-WAF to separate the addresses below 32K into eight 4K blocks. Decoder U570 is enabled when a valid address (WVMA HI) below 32K (address bit WAF LO) is placed on the memory address bus by either the Waveform μP or the System μP. The next three lower address lines (WAE, WAD, and WAC) determine which one of the eight outputs of the Decoder will be selected. Table 3-4 illustrates this address decoding.

ADDRESSES 0000h-1FFFh. Accesses in this 8k Block are mapped to U350, the Save RAM. fHU570, a 1-of-8 decoder, outputs a LO at either Y0 or Y1 for all addresses within this block and HIs on Y2-Y7. A LO at either Y0 or Y1 causes AND-gate U580C (functioning as a negative-logic OR gate) to output a LO $\overline{\text{SAVE}}$ enable. This LO is inverted twice via Q244 and Q332 and holds the chip-select input of Save RAM U350 enabled LO. Since this address block is the only block that accesses the SAVE memory, when other address blocks are decoded by U570 (in the descriptions to follow), Y0 and Y1 are HI and U350 disabled via Q244 and Q332.

NOTE

The chip-select circuit between the $\overline{\text{SAVE}}$ output of U580C and RAM U350 is identical to that for the System μP RAM (U664, diagram 1). The circuit determines chip selection during normal operation and isolates the Save RAM chip-select input when power is off. See the descriptions in "Battery" and in "Battery-Backup for Save Memory" for more information.

The Save RAM is divided into four 8K pages with only two pages used. Since the 0000h-1FFFh addresses can only address 8K of memory, the two bits, SVPG0 and SVPG1, select which 8K page the 0000h-1FFFh addresses (an 8K address block) map to by controlling address bits AD and AE of U350. These lines, in turn, are controlled by the two lower Waveform Data Bus bits WD0 and WD1 via the Interrupt Latch U550.

Normally, SVPG0 and SVPG1 are always set HI allowing the 8K address block to always address the same page. However, when the Vertical mode is ADD or MULT at the same time the Acquire mode is ENVELOPE, additional Save memory space is required. Therefore, the Waveform μP will switch those lines LO to select another page as required. The System μP also switches those lines via the Waveform Data Bus when running internal diagnostic checks on the Save RAM.

Writing to or reading from any of the Waveform μP RAM space is done via bidirectional Bus Buffer U352. When Save RAM U350 is selected by the $\overline{\text{SAVE}}$ line going LO, U352 is also enabled via AND-gate U580D. The state of the $\overline{\text{WWR}}$ (waveform write) control line determines the direction of the data transfer.

ADDRESSES 2000h-4FFFh and 6000h-6FFFh. Addresses in these ranges select either Y2 ($\overline{\text{DISP}}$), Y3 ($\overline{\text{DATT}}$), Y4 ($\overline{\text{ACQ}}$), or Y6 ($\overline{\text{WHMMIO}}$). $\overline{\text{DISP}}$, $\overline{\text{DATT}}$, and $\overline{\text{ACQ}}$, are used to select the Display and Display Attribute Memories (diagram 16) and the Acquisition Memory (diagram 8) respectively. WMMIO (Waveform Memory-Mapped I/O) is used to select the Register Decoding Circuitry.

With the output of U580C HI for all accesses in this group, Y0 and Y1 hold Save RAM U350 disabled (see "ADDRESSES 0000h-1FFFh" discussion). The HI $\overline{\text{SAVE}}$ also holds the input to U580D HI; the other input to U580D is held HI by the output of U432A. The output of U432A is HI because one of its inputs is held HI by Y5 and the other held HI by Y7 (via OR-gate U132C). The HIs at both inputs to U580D hold the Waveform Data Buffer disabled for all accesses in this group.

When WMMIO (6000h-6FFFh) is decoded LO, decoder U540 is enabled. U540 operates similarly to U570 and uses address lines WA0-WA4 to produce its various I/O enabling outputs. Address bits WA3 and WA4 are used as chip selects and cause the output of U540 to fall into the

Table 3-4
Waveform μP Address Decoding

ADDRESS BITS			OUTPUT SIGNAL (Active LO)
WAE	WAD	WAC	
LO	LO	LO	(Y0 or Y1) SAVE from NAND-gate
LO	LO	HI	U580C to enable the SAVE memory.
LO	HI	LO	(Y2) DISP—Selects display memory.
LO	HI	HI	(Y3) DATT—Selects attribute memory.
HI	LO	LO	(Y4) ACQ—Selects acquisition memory.
HI	LO	HI	(Y5) WPCMDN/COEFF—Selects either the command or the coefficient memory.
HI	HI	LO	(Y6) WMMIO—Enables Waveform μP memory-mapped I/O Decoder U540.
HI	HI	HI	(Y7) WPRAM2—Decoded to enable waveform processor RAM U440.

eight locations immediately above those of Decoder U884 (diagram 1) for System μP memory-mapped I/O.

The outputs of U540 allow the accessing processor to read the display status ($\overline{\text{SSREG}}$), to read the two-byte address of the last-acquired point ($\overline{\text{RDMAR0}}$ and $\overline{\text{RDMAR1}}$), or to latch the present interrupt status ($\overline{\text{COMREG}}$). (See the "Display Status Register" and "Interrupt Latch" descriptions for further explanation.)

ADDRESSES 5000h-5FFFh. This 4K block of addresses is decoded as an access to the Waveform Processor Coefficient-Temp Memory in RAM U440. With a 5XXXh address, U570 decodes WPCMDN COEPF LO and sets its other 7 outputs HI. The LO at the input to AND-gate U432A holds its output LO, and this LO holds U440 enabled for access. (The HI $\overline{\text{SAVE}}$ disables U350 as previously described).

The LO at the output of U432A is also coupled to the input of U580D. With a LO at the input to this AND-gate, its output is LO and U352, the Waveform Data Buffer, is enabled to connect the Waveform Data Bus to the Waveform Processor RAM.

ADDRESSES 7000h-7FFFh. Addresses in this range select WPRAM2 LO. Assuming BUSGRANT and WPRAM are both LO at the inputs to XOR-gate U130A, both inputs to OR-gate U132C are LO and its output is also LO. This LO forces the output of U432A LO and enables U440 RAM. The same LO also enables the Waveform Data Buffer via U580D to connect the Waveform Data Bus to the Waveform Processor RAM.

The System Processor can also access this address bus by asserting BUSGRANT and WPRAM HI. The two HI inputs to XOR-gate U130A produce a LO at its output. The Waveform Data Buffer is enabled and the Waveform Data Buffer are enabled as was just described for the Waveform Processor access for this address group. BUSGRANT disables the Address Latches for the Waveform Processor and is inverted to enable the Bus Connect Circuitry to connect the System Address Bus to the Waveform Address Bus. The Bus Connect Data Buffer is enabled to connect the System Data Bus to the Waveform Data Bus.

Waveform μP RAM

The Waveform μP RAM is used for storage and manipulation of waveform-display data. The RAM space is divided up into four memories consisting of the 32K-×-8-bit "Save Memory" RAM space, the 2K-×-8-bit "Command-temp" RAM space, the 2K-×-8-bit "Coefficient" RAM space, and the "Interpolation" RAM space.

The 32K-×-8-bit Save Memory, U350, is where the Waveform μP places acquired waveform data that should be retained with power off. Waveforms stored in the Save RAM are retained for up to three years at room temperature with the power off by the Battery Backup System (see "Battery" in this section.

The 8K-×-8-bit RAM, U440, is where the Command-Temp, Coefficient, and Interpolation RAM spaces reside. The Waveform μP uses the Command-Temp RAM space for storage of commands to the Waveform μP from the System μP and for temporary scratch-pad storage of display calculations in process. The Coefficient RAM space

is used only for further scratch-pad storage. Interpolation RAM is used for storing interpolation calculation used for the MEASURE feature of this scope.

Reading from and writing to the Waveform μP RAM selected by the Address Decode circuit are controlled by the $\overline{WRD}$ (waveform read) and $\overline{WWR}$ (waveform write) signals respectively.

RAM Buffer

The RAM Buffer U352 allows data transfers to and from the Waveform μP RAM to take place. The buffer is enabled by U580D when any of the Waveform μP RAM locations are addressed. Buffer direction is determined by the $\overline{WWR}$ level.

Battery-Backup for Save Memory

The waveforms stored in Save Memory U350 are maintained when the power is off. The Battery-backup Circuit previously described provides supplies power to Save RAM U350, as well as System RAM while power is off. For operation of this circuit see "Battery" in this section for more information.

As was true for the chip-select circuitry for System ROM, undefined operations on the address bus can cause the chip-select circuit enable U350 as the power supplies are brought up at power-on. To prevent this, the base circuit of Q332 through diode CR244. This LO keeps the transistor biased off and U350 is disabled until the power-up $\overline{RESET}$ signal returns HI; at which time the data on the address bus is stable.

Display Status Register

Display Status Register U542A allows the controlling processor (System μP or Waveform μP) to read the status of the Display System operations. The address-decoded $\overline{SSREG}$ (sub-system status register) line from Decoder U540 enables buffer U542A to place the DISDN (display done) and ACQDN (acquisition done) signals on the WD bus where they may be read. These status bits are used by the reading μP to determine when to execute the next phase of a display or acquisition sequence.

Interrupt Latch

The Interrupt Latch (U550) allows the Waveform μP operations to interrupt the System μP for servicing and, when servicing is completed, allows the System μP to reset the interrupt.

To write data into the latch, the controlling μP addresses location 6019h, causing the $\overline{COMREG}$ line from U540 to enable U550. Data from the WD bus is written into the latch on the rising edge of the $\overline{WWR}$ pulse. The Q output from pin 10 (MDISDN) of the latch is applied to AND-gate U580B (diagram 1) where it either masks the DISDN (display done) interrupt from the System μP when it occurs or lets the interrupt pass. Masking the DISDN interrupt from the System μP permits the Waveform μP to have first access to the Display System for display updates before the System μP sees that the Display System is finished with its last task. The Q output bit on pin 15 is the WPDN (waveform processor done) interrupt and provides the Waveform μP with a way of telling the System μP that it is done with its assigned task and is ready to accept another. The output bit on pin 15 is applied to Display Status Register U542A and is used for write-readback verification of U550 and U542A during the self-check and other diagnostic routines.

The other two Q outputs, SVPG0 and SVPG1 at pins 2 and 7 respectively, control which of four 8K pages is selected when Save RAM U350 is accessed. See "Address Decode" earlier in this section for more information.

FRONT PANEL PROCESSOR

The Front Panel Processor (diagram 3) monitors the settings of the pots and switches of the Front Panel (diagram 4) and the Auxiliary Front Panel (diagram 6). The Front Panel μP allows quick system response to changes in front-panel settings without excessive use of time by the System μP. The Front Panel Processor system consists of the microprocessor integrated circuit with a built-in RAM, ROM, and A/D converter (for digitizing the potentiometer wiper voltages); the handshake logic between the System μP and the Front Panel μP (to synchronize data transfer between processors); and the data bus interface to provide the actual data transfers between busses.

Front Panel μP

Front Panel μP U700 does the reading of the front-panel pots and switches. It continuously scans the front-panel control settings and compares them against the values stored in its internal RAM. When a change is detected, the Front Panel μP issues an interrupt to the System μP. The System μP then handles the interrupt and reads the changed data from the Front Panel μP to update its control-setting values. The Front Panel μP also updates the current value list stored in its RAM for further use.

Front Panel μP U700 is externally clocked by the 4 MHz system clock applied to the external clock input (EXTAL). Initially, the LO state of $\overline{FPRESET}$ on the INT_2 input (pin 18) will clear all the internal registers of the Front Panel μP. When $\overline{FPRESET}$ goes HI, the μP executes the power-up self-test instructions stored in ROM space within the μP integrated circuit. When the self test has completed, the Front Panel μP sends the diagnostic result byte to the System μP and branches to its main program. The

main program routine sets up the data direction for the various port lines, sets the AN0-AN3 (analog inputs 0-3) to their analog input mode, and receives the eight front-panel configuration bytes from the System μP that define the manner in which the various front-panel switches and pots operate. It then begins scanning the front-panel pots and switches for their initial settings. After the initial values are determined and stored, the Front Panel μP sends those coded values back to the System μP in an 11-byte message (10 data bytes plus an end-of-message byte) to update the front-panel information held by the System μP. It then begins scanning the front-panel controls for changes from the currently stored front-panel values.

To read front-panel pot settings, the internal A/D converter of the Front Panel μP performs an 8-bit, successive-approximation conversion of the analog levels applied to the AN0 and AN2 inputs by a selected potentiometer. These analog input signals come from 8-input analog multiplexers U902 on the Front Panel (diagram 4) and U600 on the Auxiliary Front Panel (diagram 6). A specific pot to be read is selected by the multiplexer under control of the MUXSEL0, MUXSEL1, MUXSEL2, and MUXINH (multiplexer inhibit) output lines from the Front Panel μP. These select signals, in combination with the selected A/D (AN0 or AN2) input, define the pot being read. The voltages monitored on the AN1 and AN3 analog inputs are also digitized by the internal A/D converter to detect Main board temperature (MBTEMP) changes (not used at this time) and if lithium backup battery BT800 (diagram 1) is either low (needing replacement) or being charged (not allowed).

To read the front-panel switches, the Front Panel μP first sets one of the front-panel switch-matrix rows LO, using the MUXSEL0-MUXSEL2 outputs. It then sets its S/$\overline{L}$ (shift/load) output on pin 29 LO. The LO does a parallel load of the switch-closure data into shift registers U904 (diagram 4) and U700 (diagram 6). The shift/load line is then set HI (shift mode), and eight shift clocks (SHCLK) are generated to move the switch-closure data serially onto the SW OUT (front-panel switch data out) or the SW OUT A (auxiliary front-panel switch data out) lines, where it is read by the Front Panel μP. This cycle is then repeated for the seven remaining rows of the matrix to read all the switches.

When the Front Panel μP detects a change in either a switch or a pot setting from its currently stored values, it places a code identifying which control setting changed on its PA0-PA7 outputs, and it then sets the WRTOHOST (write to host) signal HI to clock Handshake Logic flip-flop U861B. The resulting HI on the Q output of the flip-flop is the front-panel interrupt (FPINT) to the System μP, telling it that the front-panel settings have been changed.

The System μP handles the interrupt by reading the byte from the Front Panel μP; and then, via the Handshake Logic, it resets flip-flop U861B to remove the interrupt and set HOSTDNRD (host done reading) HI. This signals the Front Panel μP that the System μP has read the code identifying the changed control. The Front Panel μP then places the new control-setting value on its output bus and reasserts the front-panel interrupt using the WRTOHOST line to again clock flip-flop U861B.

The System μP then reads the changed-data bytes for the identified control(s) (either three bytes or five bytes depending on whether one or two control changes are being sent) and reasserts HOSTDNRD. Changes of up to two controls are remembered by Front Panel μP U700 so that if the System μP is busy, the control changes are not lost while the Front Panel μP is waiting to make the transfers. If more than two controls are changed before the System μP has time to read the changes, the oldest change is written over and lost.

The $\overline{\text{WRTOFP}}$ (write to front-panel processor) input to U700 at pin 3 is set LO (via the Handshake Logic) when the System μP wants to input data to the Front Panel μP. The Front Panel μP then reads one byte of data from the System μP in a manner similar to that just described for transfers from the Front Panel μP to the System μP. This mode allows the System μP to change the current control configuration list stored in the limited RAM space of the Front Panel μP. This list defines how the operation of pots and switches is to be interpreted (for example, momentary contact or toggle switches).

Jumper J155, connected to the PC_7 and PD_7 inputs, is used to enable diagnostic test routines that verify functionality of U700. The test routines may also be used to troubleshoot the Front Panel Processor system. These tests are explained in the Diagnostics portion of the "Maintenance" section of this manual.

Handshake Logic

The Handshake Logic circuit, formed by NOR-gates U862A, B, C, and D and flip-flops U861A and B, controls and synchronizes data transfers between the System μP and the Front Panel μP.

Data transfers between the two processors are initiated by interrupts that signal the destination processor that service is requested. When the Front Panel μP has changed-value data to give to the System μP, it will place the data

bytes to be given to the System μP on its PA_0-PA_7 (port A—bits 0 through 7) outputs. It then asserts WRTOHOST (write to host) HI, clocking the FPINT (front-panel interrupt) at the Q output of U861B HI.

Depending on what the System μP is doing, it may either service the interrupt request immediately, or it may wait for time to be available. When it responds to the interrupt, it does a read of the Front Panel "register" at address 6209h. The decoded $\overline{\text{FPREG}}$ signal from Trigger Holdoff Decoder U781 (diagram 12) allows OR-gates U862B and U862C to pass the $\overline{\text{WR}}$ or $\overline{\text{RD}}$ signals. For a read, both input pins to U862B are LO, causing the output of U862A to go LO. This enables buffer U751, placing the data from the Front Panel μP on the System μP data bus (FP0-FP7) and, at the same time, resets flip-flop U861B. Resetting U861B removes the front-panel interrupt and sets HOSTDNRD (host done reading) to U700 HI.

When the System μP needs to write to the Front Panel μP, it writes data to address 6209h. This latches data from the System μP data bus into register U742. The enable to U742 is via U862C. The latch enable also resets the Q output of flip-flop U861A LO via U862D to produce the $\overline{\text{WRTOFP}}$ (write to front-panel) interrupt to U700. Latching data into U742 immediately frees the System μP to resume other tasks, since it doesn't have to wait for the Front Panel μP to service the interrupt.

When U700 services the interrupt by the System μP, it sets $\overline{\text{FPRD}}$ (front-panel reading) LO and enables the latched data in register U742 onto the Front Panel data bus. It then reads the data into its internal registers and asserts FPDNRD (front-panel done reading). FPDNRD going HI clocks the $\overline{\text{FPDNRD}}$ status bit from flip-flop U861A pin 6 HI to signal the System μP that it is done reading the byte and removes the $\overline{\text{WRTOFP}}$ interrupt present on U861A pin 5. Each data byte transfer from the System μP to the Front Panel μP and vice versa is done using the two handshake routines just described.

Trigger Status Indicators

The Front Panel Trigger Status Indicators provide visual information regarding trigger slope and trigger status to the user. Data written to LED Register U741 from the System μP turns on the LED that reflects the current trigger status. A LO output from U741 turns on the associated LED. The LED Register is enabled by a System μP write to address 6208h. Trigger Holdoff Decoder U781 (diagram 12) produces the decoded $\overline{\text{LEDREG}}$ signal that enables data at the input pins to be latched when the $\overline{\text{WR}}$ clock goes HI.

FRONT PANEL CONTROLS

The Front Panel is the operator's interface for controlling the user-selectable oscilloscope functions.

All of the Front Panel controls (diagram 4) are "soft" controls in that they are not connected directly into the signal path. Therefore, associated circuits are not influenced by the physical parameters (such as capacitance, resistance, and inductance) of the controls. In addition, converting the analog output levels of the potentiometers to digital equivalent values allows the System μP and the Front Panel μP to handle the data in ways that enhance control operation.

The variables defining the current settings of the control pots and the front-panel switches are stored and continually updated in Nonvolatile RAM U664 (diagram 1) by the System μP. The data remains stored when the oscilloscope is turned off so that when the scope is turned on again the System μP returns to the same front-panel setup that was present when the scope was turned off.

Front-Panel Switch Scanner

The Front Panel switches are arranged in an electrical array of eight rows and six columns. Switches are placed at row-column intersections, and when a switch is closed, one of the row lines is connected to one of the column lines through an isolation diode. Checking for switch conditions (open or closed) is done by setting a single row line LO and then sequentially checking the six columns to determine if a LO is present on any of the column lines. After each column line in a row is checked, the current row line is reset HI and the next row line is set LO to check the next six columns. A complete check of the front-panel switches consists of setting all eight row lines LO in order and performing a six-column scan for each column to check for a LO.

A row is selected for checking by the Front Panel μP (U700, diagram 3) when it switches the MUXSEL lines (0-2) applied to multiplexer U903 to set a row line LO. To check the columns, the processor pulses its S/$\overline{\text{L}}$ (shift/load) select line to shift register U904 first LO and then HI. This causes a parallel load of the six column-line bits (plus the seventh and eighth bits tied HI by R934) into the shift register. The processor then generates eight shift clocks (SHCLK) to U904, serially shifting the switch data out on the SWOUT (switch data out) line. The serial data bits are applied to the PB0 input (pin 25) of the Front Panel μP to be checked. Any LO bits in the column-line data tell the μP that a switch is closed. Since the Front Panel μP knows which row line it set LO, it can determine from the position of the LO bits in the serial data string which of the switches are closed.

In addition to the front-panel push-button and continuous-rotation switches connected in the switch array, there is a rate switch associated with the Horizontal Position, the CH 1 Vertical Position, the CH 2 Vertical Position, and the Cursor Position potentiometers. These switches are normally closed in the center positioning range of the associated pot. When the pot is rotated in either direction out of this range, the rate switch opens. The open switch signals the Front Panel μP that the associated control function has changed from normal (absolute) positioning to a faster, rate-change positioning mode. Rotating the pot still further into the rate region causes the associated on-screen display position to change at a still faster rate. When the pot position is returned to its center range (rate switch closed), further positioning of the associated display occurs from where the rate function positioning left off.

Pot Scanning

The Pot Scanning circuitry, working together with the A/D converter internal to Front Panel μP U700, produces digital values for the wiper voltages of the front-panel potentiometers and for the voltages monitored by the auxiliary front-panel circuitry. Analog multiplexer U902 selects which of the eight front-panel pots are read. (Trigger Level control R902 and Holdoff control R901 are continuous-rotation potentiometers made up of two separate resistive elements each.) Analog multiplexer U600 (diagram 6) selects the auxiliary front-panel value to be read.

Three MUXSEL control lines to multiplexers U902 and U600 select the pot or value to be read. The analog voltage level at the wiper of the pot selected by U902 is output at pin 3 (AOUT0) and is applied to the Front Panel μP at pin 21 (analog input AN0). Analog voltages selected by multiplexer U600 are applied to analog input AN2. The voltage levels at these inputs are digitized, and the amount and direction of changes from the previously stored values are calculated. Changed values are stored in the internal RAM of U700 for comparison during future scans, and the change data is then relayed to the System μP. That change data is used by the System μP to update its current control settings and pot values list and to update the front-panel variables in Nonvolatile RAM U664.

SYSTEM DAC AND ACQUISITION CONTROL REGISTERS

The System DAC and Acquisition Control Registers circuitry (diagram 5) is used to set various analog reference voltages throughout the instrument and controls such things as preamplifier gain, vertical position and centering, trigger levels, holdoff time, common-mode rejection, graticule illumination, and CCD offsets.

The System DAC portion of the circuitry consists of a data latch that stores the digital value to be converted, a D/A converter that does the actual conversion, a multiplexer system to route the resulting analog voltage to the proper control circuit, and a sample-and-hold system that stores the analog levels between updates. Much of the multiplexing and sample-and-hold circuitry is shown in diagram 6, System DAC (cont) and Auxiliary Front Panel.

The other portion of diagram 5 is the Acquisition Control Registers circuitry, used by the System μP to set up the acquisition and triggering modes. The System DAC portion is described first.

D/A Converter

The D/A Converter stage, U860, converts the digital value written into registers U850 and U851 by the System μP into two complementary output currents. (Complementary in this case means that the sum of the two currents equals a predefined value.) The digital data bits to be converted are serially clocked into the shift register from data bus line D7 (via U280). Sixteen data bits are sequentially placed on data bus line D7 and clocked into the shift register on the rising edges of 16 $\overline{WR}$ pulses (clock is via U280A and U280B). As the bits are being loaded into the registers, the DAC output current does not correspond to any useful value, but the multiplexers used to direct that output to the following stages are not enabled during loading. After all 16 bits have been clocked into the register, the inputs to DAC U860 will be at their proper levels and the DAC outputs will be valid levels. One of the multiplexers may then be enabled by the System μP using the DAC MUX enables via register U272.

Only the first 12 bits (DAC0 through DAC11) of the 16 bits loaded into the registers for are used for conversion data. The next three higher bits are used as 1-of-8 select bits to the four analog multiplexers that route the DAC output voltage to the proper Sample-and-Hold circuit. And finally, the MSB of shift register U851 is used in a write-readback operation that allows the operation of registers U850 and U851 to be checked by the System μP during self checks and diagnostics.

The magnitude (range) of the DAC output currents is set by the voltages applied to pins 14 and 15 of U860. Pin 15 V_{REF-} is tied to ground through R761. The reference voltage to pin 14 is applied via a voltage divider (R760 and R860) between the +10 V_{REF} supply and the output of the DAC Gain Sample-and-Hold, U660. The System μP enables self-calibration of the gain of U860 via this Sample-and-Hold circuit. Gain changes are explained in the discussion of the DAC Gain Self-Calibration circuit.

DAC I-TO-E CONVERTER. This circuit changes the differential output currents from DAC U860 into a single-ended output voltage that is routed to a selected Sample-and-Hold circuit via one of the analog multiplexers.

The output currents from DAC U860 develop a voltage drop across the resistive networks at the inputs to operational amplifier U661C. The equivalent input impedance at both inputs is approximately 200 ohms; so, when both currents are equal (middle range of the DAC), the output voltage of operational amplifier U661C will be close to zero volts. An offset current is added to the non-inverting input node via R666 to precisely set the midrange value to zero volts. The gain of U661C is set by the ratio of R663 to R664, and the (calibrated) output voltage ranges from −1.36 V to +1.36 V.

DAC OFFSET. The DAC Offset level is self-adjusting and is updated via DAC Offset Sample-and-Hold U650 each time the DAC System cycles through its DAC channels to update its control levels.

At the beginning of each DAC-update cycle, the System μP writes 0800h to DAC input shift registers U850 and U851; this corresponds to zero volts (center of the DAC range). The DAC output currents representing zero volts are converted by the DAC I-to-E Converter U661C to a voltage that is applied to U650 via multiplexer U651. Any deviation from the desired zero-volt level causes the output of U650 (configured as an inverting integrator) to shift slightly. This applies an offsetting voltage to DAC I-to-E Converter U661C via R666 and R665 to bring its output level back to precisely zero volts.

Capacitor C655 holds the offset level constant between update cycles (every 64 ms) to keep the proper offset for the entire DAC cycle. By updating the offset every 64 milliseconds, offset variations that would otherwise occur over time and temperature changes are eliminated.

DAC GAIN. The DAC Gain is set during each DAC-update cycle immediately after DAC Offset is set and keeps DAC gain constant with time and temperature changes.

To set the DAC Gain, the System μP loads 0F59h into DAC input registers U850 and U851 and routes the resulting output voltage to DAC Gain Sample-and-Hold U660 via multiplexer U651 pin 2. A digital input of 0F59h to the DAC is supposed to produce an output of +1.25 V from U661C. The resulting DAC output is compared to a +1.25 volt reference by operational amplifier U660. Any deviation from the correct +1.25 V level produces a gain-correction voltage applied to the DAC via R760. Capacitor C662 maintains the correction voltage between DAC update cycles.

Multiplexer Select

The Multiplexer Select circuit, composed of addressable latch U272 and the associated decoding gates, provides the enabling signal that selects one of the four 1-of-8 multiplexers to route the DAC output voltage to the Sample-and-Hold circuits. Data applied to the D input of U272 from data bus bit $\overline{D7}$ (via U280D) is latched to the addressed output pin as determined by the logic levels on the A, B, and C select lines (A0 through A2). The input data is written to the addressed output on the falling edge of the enable signal at pin 14 (via U280A and U280C). The logic state written to the output remains latched when the enable signal returns HI. The states of the unaddressed outputs remain unchanged. To enable the latch, NOR-gate U280A (functioning as a negative-logic NAND-gate) needs the $\overline{\text{DACSEL}}$ (DAC select) line LO to produce a HI output. That HI is inverted by U280C to enable the Multiplexer Select register to be written into. That same LO $\overline{\text{DACSEL}}$ is applied to NOR-gate U280D to enable it to pass the data on the D7 line to the D input of U272 and to the DAC input register, formed by U850 and U851.

Multiplexer U651, when enabled by Multiplexer Select Latch U272, routes the analog output voltage from DAC I-to-E Converter U661C to one of eight Sample-and-Hold circuits, depending on the output specified by the logic states on the its select inputs. Selection is determined by three bits clocked into DAC Register U851 as described in the preceding D/A Converter discussion. One of three other multiplexers, shown in diagram 6, may be enabled instead of U651 to pass the DAC output to one of the Sample-and-Hold circuits on their outputs (also shown in diagram 6).

Sample-and-Hold

The eight Sample-and-Hold circuits shown on diagram 5 (formed by U641A through U641D, U650, U660, U661A, U661B and their associated components) store and buffer the analog voltage levels directed to them by multiplexer U651. Each of the operational-amplifier circuits selectable by U651 (except the DAC Offset and DAC Gain operational amplifiers, U650 and U660 respectively) has a hold capacitor on one input that is charged up to the DAC output voltage level through the selected multiplexer channel. When the multiplexer channel is then deselected, the capacitor holds the voltage at a fixed level so that the associated Sample-and-Hold circuit provides a steady voltage level to the circuit it controls. Voltage gain of the Sample-and-Hold operational amplifiers range from more than 4.5 in the CH 1 and CH 2 Gain-Cal circuits down to 2 in the

Jit 1 Gain and Jit 2 Gain amplifiers and down to about 1 for the CH 1 and CH 2-BAL voltage followers. The Jitter Gain circuits (formed by U661A and U661B) produce a negative 5 V dc offset voltage at their output pins as their gain-setting resistors are referenced to the +5 V supply. The DAC Offset and DAC Gain Sample-and-Hold circuit operations are described in the previous D/A Converter discussion.

Acquisition Control Registers

Mode control of the analog acquisition system and trigger circuitry is controlled by the System μP via shift registers and a decoder. The System μP, through its address decoding circuitry, enables Decoder U271 to produce a shift register clock at one of its eight outputs. These clock signals are used to move serial data from the ACD (acquisition control data) line, U272 pin 5, into one of the various Acquisition Control Registers, of which three are shown in diagram 5. They are Peak Detector Control Register U530, Gate Array Control Register U270, and Trigger Source Control Register U140. Other registers clocked are the Channel 1 and Channel 2 Control Registers (U510 and U220 on diagram 9), the internal control registers of the CH 1 and CH 2 Preamplifiers (U420 and U320 on diagram 9), and the internal control registers in the A/B Trigger Generator (U150, diagram 11).

The ACD line is shared by all the Acquisition Control Registers; the selected clock determines which register will be loaded with the data being written by the System μP. Decoder U271 is enabled when the $\overline{\text{ACQSEL}}$ and $\overline{\text{WR}}$ lines are LO and address line A3 is HI. Address lines A0, A1, A2 determine which of the output lines produces the clock signal. A data bit present on the ACD line (previously written to latch U272 in a DAC write cycle) is loaded into the clocked register on the rising edge of the $\overline{\text{WR}}$ signal as U271 becomes unenabled and its selected LO output goes HI. Each bit to be loaded must be successively written to U272 then moved into a register by the output clock from U271.

SYSTEM DAC (cont) AND AUXILIARY FRONT PANEL

The DAC multiplexing and sample-and-hold circuits included in diagram 6 operate similarly to those described in the DAC System (diagram 5) discussion. The analog voltage output from the DAC I-to-E Converter is routed through one of the three additional multiplexers (shown in diagram 6) to several types of hold circuits.

DAC Multiplexers

DAC Multiplexers U821, U830, and U831 route the analog output voltage from DAC I-to-E Converter U661C (diagram 5) to the various Sample-and-Hold circuits. Operation of each multiplexer is identical to that of Multiplexer U651, previously described in the System DAC circuit discussion. Each multiplexer is individually enabled by a bit from Multiplexer Select Latch U272, and signal routing through the enabled device is controlled by the three select bits applied to it from the three most significant bit outputs of DAC Register U851.

Sample-and-Hold

A separate Sample-and-Hold circuit is associated with each of the multiplexer outputs. An analog voltage routed from the DAC I-to-E Converter through the selected multiplexer channel charges up the hold capacitor at the input of an operational amplifier in the selected Sample-and-Hold circuit. When that multiplexer channel is deselected, the voltage level is held on the capacitor because of the high-impedance discharge paths presented by the multiplexer output and the operational amplifier input. The individual operational amplifiers are configured as buffers with voltage gains varying from −0.47 to +10, depending on the requirements of the function that is being controlled. The CH 1 and CH 2 Position Sample-and-Hold circuits also provide a dc offset of their output levels to properly bias the inputs they drive.

Cal Signal Amplifier

The Cal Signal Amplifier (U610) operates in a manner similar to the Sample-and-Hold circuits just described. It is used to supply test signals to the CAL inputs of the CH 1 and CH 2 Peak Detectors (U440 and U340, diagram 10) for Self Calibration of the acquisition system. The test signal level, stored on capacitor C733, is applied to the input of an amplifier internal to U610 which has dual-differential outputs. The complementary-current outputs for each channel are approximately 6 mA ±1.25 mA.

Z-Axis Control

The Z-Axis Control stage consists of Q810, U811, U810A, U810B, five-transistor array U812, and associated components. Multiplexer U811 selects one of three intensity-control voltages—normal, intensified, or readout (output from Sample-and-Hold buffers U820B, U820C, or U820D) and routes it to a current source composed of U810A, U810B, and Q810. The amount of current passed by Q810 controls the display intensity. The transistors in array U812 form an automatic gain compensation circuit for Z-Axis Amplifier U227 (diagram 19).

Selecting an input to pass through multiplexer U811 is done by two active input signals, BRIGHTZ and RO. (The third select input is a permanent LO, so one of the first four inputs only can be selected.) For normal-intensity waveform displays, all select bits will be LO to select input 0 to switch through U811. If the waveform display should be intensified at any time, the BRIGHTZ input will go HI, selecting input 1. When readout is to be displayed, the RO input will go HI, selecting either input 3 or input 4, depending on the setting of the BRIGHTZ bit. Since inputs 3 and 4 are both connected to the INT-RO (readout intensity) control voltage level, the readout displays are not intensified.

The selected intensity control voltage is applied to U810B, configured as an inverting buffer with a gain of −1. The output voltage is offset −4.06 V by the voltage divider at pins 3 and 5 of U810 (R814 and R815) and resistor R816 at pin 6. The resulting inverted and shifted output is converted to a current by R812 and applied to the emitter of Q810.

The circuitry of operational amplifier U810A and transistor Q810 is arranged so that the transistor is on with its emitter held at −2.7 V. The −2.7 V level at the emitter is set by the bias on input pin 3 of operational amplifier U810A. The voltage developed at the output of U810B causes a current to flow in R812 and sets the current drive level for the Z-Axis circuit (diagram 19). This Z-INT drive current supplied via U812E from pin 14 may vary from 0 mA to 4 mA (−1.36 V to +1.36 V respectively at the output pin of multiplexer U811).

When the intensity of the selected display is at minimum, the output control voltage from multiplexer U811 will be below −1.36 V. This causes the output of U810B to go to approximately −2.7 V, reducing the emitter current to Q810 to approximately zero. Diode CR810 limits the reverse-bias voltage across the base-emitter junction of Q810 to about 0.6 volts and protects the base-emitter junction from excessive voltage.

Automatic compensation of the Z-Axis Amplifier gain is carried out in five-transistor array U812. Transistors U812B and U812C form the bias network for U812D, one-half of the Z-Drive compensation amplifier. Biasing for the other transistor of the differential pair is supplied by U812A, R817, and a resistor internal to the Z-Axis Amplifier that is tied to the +5 V_D supply. The differential amplifier pair is biased so that the total current is divided between the two sides. The resistance value of the internal resistor in the Z-Axis Amplifier is an indication of the gain of that device. Changes in that value that occur between different Z-Axis Amplifiers shift the biasing level of U812E to either increase or decrease the share of the total current through that transistor by a small amount. The change in current is in the appropriate direction to make the display intensity of different instruments comparable with exactly the same Intensity control settings. Capacitor C817 bypasses high-frequency noise present on the ZGAIN signal line.

The SPOTWOB (spot wobble) signal line, at the output of Operational Amplifier U810B, picks off the various intensity levels. Those levels are used in the Horizontal and Vertical Output Amplifiers (diagram 18) to dynamically correct intensity-related position shifts on the crt (described in the Display Output circuitry discussion).

Graticule Illumination

The Graticule Illumination circuit, composed of U820A, U520G, and associated components, sets the brightness of the three lamps used to light up the graticule lines etched on the crt faceplate.

Operational amplifier U820A is configured as an inverting integrator. Inverting buffer U520G may be thought of simply as an open-collector transistor following operational amplifier U820. The circuit appears this way because the negative feedback around the loop via U820 and voltage divider R824-R825 keeps U520G in its linear operating range. Gain around the loop (11) is set by the ratio of R822 to R823 plus 1. The DAC control voltage applied to pin 2 of U820A causes the integrator output to slowly ramp in the opposite direction. This output is inverted by U520G, and it sets the current in the graticule lamps. Between DAC-updates no integration takes place, and the charge held on C822 holds the output of the inverting buffer, and thereby the graticule lighting, constant.

Auxiliary Front Panel

The Auxiliary Front Panel circuitry provides a means of reading the front-panel bezel push buttons, located directly below the crt, as well as several analog voltages associated with the front-panel BNC input connectors. The circuit consist of analog multiplexer U600 (used to route the various analog voltages to the A/D converter), parallel-loading shift register U700 (used to relay switch-closure data to the Front Panel μP, shown in diagram 3), and associated components.

Analog multiplexer U600 routes one of the eight input levels to the A/D converter internal to Front Panel μP U700 (diagram 3), depending on the three-bit code applied to its select inputs. The selected signal may be one of the four probe-coding voltages (developed by the voltage divider formed by the encoding resistance of the probe attached to the input connectors and the associated pull-up resistor within R601), the CH1 OVL (overload) or CH2

OVL levels (used to indicate when an excessive voltage is applied to the input connector), or one of the two, 180 degree out-of-phase wipers on the Intensity control (a continuous-rotation pot).

Auxiliary Switch Register U700 performs a parallel load of the status of all of its input bits whenever the Front Panel μP puts out a SHCLK (shift clock) with the S/$\overline{L}$ (shift/load) select input of the register set LO. Once loaded, the S/$\overline{L}$ input is set HI, and the eight bits of switch-closure data are clocked out to the Front Panel μP on the SWOUTA (switch data out-auxiliary Front Panel) line with eight more clocks applied to the clock input of the Auxiliary Switch Register. Switches read include the five menu select switches on the lower edge of the crt bezel, the Intensity Control SELECT switch, the STATUS switch, and the MENU OFF/EXTENDED MENU switch.

SYSTEM CLOCKS

The System Clocks circuitry (diagram 7) produces the fixed-frequency System clocks signals used throughout the oscilloscope. These clocks are developed from a 40 MHz master clock frequency, and they are used to drive state machines that produce other special-purpose clocks that control the waveform acquisition processes.

Master Clock

The Master Clock circuit produces 20 MHz and 8 MHz clocks ($\overline{C20M}$ and C8M) by dividing down the output from the 40 MHz crystal oscillator circuit, Y611. The oscillator circuit drives both the divide-by-two flip-flop (U612A) and the divide-by-five circuit (flip-flops U612B, U615A, and U615B) in parallel via inverter U513A. The 20 MHz clock is obtained from flip-flop U612A. With its Set, Clear, J, and K inputs all held permanently HI, the flip-flop toggles on each negative-going 40 MHz clock edge to divide the input clock frequency by two.

The divide-by-five circuit is a state machine formed by J-K flip-flops U612B, U615A, and U615B. With the two feedback signals to the J and K inputs of U612B, the flip-flop chain sets logic level on the J and K inputs of U615B that allows its Q output to change states only every five 40 MHz input clocks to produce the 8 MHz clock.

Jumper J132 allows an external clock signal to be substituted for the 40 MHz clock signal to aid in testing and troubleshooting.

Secondary Clocks

The Secondary Clocks circuit further divides the 20 MHz clock to produce other system clock rates. The flip-flops within U710, along with logic gates U711A, U711B, U711C, and U712B, produce 10 MHz, 5 MHz, and 2.5 MHz clocks.

Flip-flop U710D and exclusive-OR gate U711C generate the 2.5 MHz clock (CLK3A) that is delayed 3/8 of a cycle (150 ns) with respect to the 2.5 MHz clock at the 3Q output (CLK1A). CLK1A, CLK2A, and CLK3A are used for control-clock generation in the Waveform Processor system (diagram 2). The 10 MHz clock is the reference signal to the Phase Clock Array's phase-lock loop circuit (U381, diagram 11). This clock is available at J133 for use as a trigger signal when troubleshooting the Waveform Processor system with a logic analyzer or test oscilloscope.

The CLK1A, CLK2A, and CLK3A clocks are buffered by U712A, U712C, and U712D to the Waveform μP. Buffering these clocks ensures that a fault on the buffered side will not halt operation of the Secondary Clock Generator circuit. Series-damping resistors R713, R715, and R716 reduce ringing in the interconnection cable. The 5 MHz clock is used in the display control circuitry, diagram 17.

Minimum-Delay 1 MHz Clock

The Minimum-Delay 1 MHz Clock circuit produces a 1 MHz clock (2XPC) whose transitions very nearly coincide with those of the 20 MHz clock. The requirements of the clock timing dictate that the delay between a rising edge of the 20 MHz clock (C20M2 on U720A pin 3) and the 2 MHz $\overline{TTL4C}$ (TTL-compatible phase 4 clock, originating from Phase Clock Array U470—diagram 11) transitions be less than 50 ns to ensure proper phasing. Since the propagation delay (2XPC-to- $\overline{TTL4C}$ delay) through the Phase-Clock Array is a significant portion of the 50 ns allowed, the phase of the 2XPC (two-times CCD "C" register clock rate) clock relative to the 20 MHz clock must be optimized for minimum delay.

To obtain minimum delay, U622, U523B, and their associated logic gating are configured as a divide-by-20 counter whose output is synchronized to the 20 MHz clock (plus propagation delay through U523B). Counter U622 and NAND-gate U620C provide division by ten, producing a 2 MHz clock (4XPC) at pin 11 of U622.

After one run through the counting cycle at power-on, any unknown counter states in divide-by-ten counter U622 are resolved, and the circuit counts in the following manner: If the circuit does not start in the Load condition, it will be in the Count mode (a HI on pin 9 from the output of NAND-gate U620C) and the 20 MHz clocks cause the counter output to increment until it reaches 1100 (binary). At this point the output of U620C will go LO, causing the counter to load the count 0011 (binary) from its inputs with the next clock. Once the counter is loaded, the output of U620C will return HI, and normal counting from a known state commences. When the counter reaches 1100 again, the load-count sequence will be repeated, requiring ten 20 MHz clocks to complete the cycle.

AND-gate U623C watches the three lowest bits of the counter outputs (Q_A, Q_B, and Q_C). The output of U623C (pin 8) will be HI during the "7" state (0111 binary) of each 10-count cycle and will stay HI for one 20 MHz clock cycle (50 ns). This HI is applied to the K input and the J input (via OR-gate U522B) of flip-flop U523B. With the K and J inputs both HI, the flip-flop toggles when the next 20 MHz clock arrives. Assuming the Q output of the flip-flop was LO, toggling to a HI applies a HI to the J input via OR-gate U522B. When the output of U623C returns LO (next 20 MHz clock), the J and K input states of the flip-flop will keep the Q output HI with subsequent 20 MHz clocks.

The Q output of U523B will stay HI until the next seven (0111) state from AND-gate U623C arrives, at which time the J and K inputs are again set HI. On the rising edge of the next 20 MHz clock the Q output of flip-flop U523B toggles LO. When the 50 ns pulse from U623C returns LO, the J and K input states will both be LO, and further 20 MHz clocks are prevented from changing the Q output state of the flip-flop. The output remains LO until the next HI state from U623C starts the divide sequence over again. Note that transitions of the 1 MHz signal (2XPC) at pin 9 of U523B are delayed from the $\overline{C20M}$ (20 MHz clock) clock rising-edge transitions by only the propagation delay through the flip-flop (about 7 ns).

CCD Output-Sample Clocks

The CCD (charge-couple devices) Output-Sample Clocks stage controls signal transfers from the Acquisition CCD-Clock Drivers (diagram 10) to the external CCD Output circuitry (diagram 14). It consists of a state machine synchronized to the 20 MHz clock (and thus the CCD events) and produces clocks to: (1) move sampled data out of the CH1 CCD array, (2) move sampled data out of the CH2 CCD array, (3) reset both the CH1 and CH2 CCD array output-charge wells in preparation for the next transfer, and (4) phase-lock the CCD-Data Clock stage. Figure 3-3 illustrates the timing of these clocks and other clocks in the System Clock Generator; it may be of use in following the discussion of circuit operation.

When acquired samples are to be shifted out of the CH1 and CH2 CCD array, the TTL version of the Phase-Clock 02 output ($\overline{TTL2C}$) from Phase Clock Array U470) will be toggling at 500 kHz. Transitions of the $\overline{TTL2C}$ clock are resynchronized to the 20 MHz clock (C20M2) by flip-flop U720A to correct the phase between the $\overline{TTL2C}$ clock and the state machine outputs. This correction closely synchronizes charge transfers within the CCD (relative to the 2XPC clock) with the signal transfers out of the CCD.

When the $\overline{SYNC2C}$ (synchronized phase-4 clock) is LO (pin 5 of flip-flop U720A), the LOAD signal applied to shift registers U730 and U830 (via AND-gate U623B and inverter U513E) will be HI. This HI, along with the HI $\overline{SYNC2C}$ signal from pin 6 of flip-flop U720A, causes both shift registers to do a parallel load of the fixed logic levels applied to their D input pins. The levels loaded set the $\overline{OS1}$ (sample CH1-CCD outputs), $\overline{OS2}$ (sample CH2-CCD outputs), and the $\overline{RST}$ (reset CCD output wells) outputs from U730, and the $\overline{SYNC}$ (sync data clocks) output from U830 all HI. The HI $\overline{RST}$ level applied back to U621 and the HI output from NAND-gate U620B will be loaded into counter U621 as 0101 binary because of the LO $\overline{LOAD}$ output of U623B applied to the CT/ $\overline{LD}$ input pin. This state then stays as is for the remainder of the LO state of the $\overline{SYNC2C}$ signal.

When the $\overline{SYNC2C}$ output of flip-flop U720A returns HI, counter U621 is enabled by the HI from AND-gate U623B to count for three, 20 MHz clock cycles (150 ns), reaching the count of 0111 binary. The next clock toggles the QC output of U621 LO (count goes to 1000 binary), and the $\overline{LOAD}$ output from AND-gate U623B is forced LO. The HI LOAD signal output obtained from inverter U513E, along with the LO SYNC2C from flip-flop U720A pin 6, sets up shift registers U730 and U830 to shift right. The next 20 MHz clock (250 ns after the 2XPC clock toggled) shifts a LO to the $\overline{OS1}$ output of U730 (pin 14) and loads a binary 0100 into counter U621 (since the output of NAND-gate U620B is now LO). The fixed HI applied to the SR data input of U730 is shifted to the Q_A output.

After 0100 is loaded into counter U621, the $\overline{LOAD}$ output of U623B returns HI (since pin 12 of U621 has been set HI by the inputs loaded into the counter). This once again produces a LO LOAD output from inverter U513E and prevents U730 and U830 from shifting. Counter U621 counts four cycles of the 20 MHz clock (200 ns), reaching count 0111. The next 20 MHz clock toggles the Q_C output of U621 LO and sets the $\overline{LOAD}$ line LO once again, enabling shift registers U730 and U830. The next clock (250 ns) shifts the previously loaded LO from the $\overline{OS1}$ output right to the $\overline{OS2}$ output of U730 and moves a HI from the SR data input into the $\overline{OS1}$ output. At the same time, counter U621 is reloaded to 0100 binary to again restart its count.

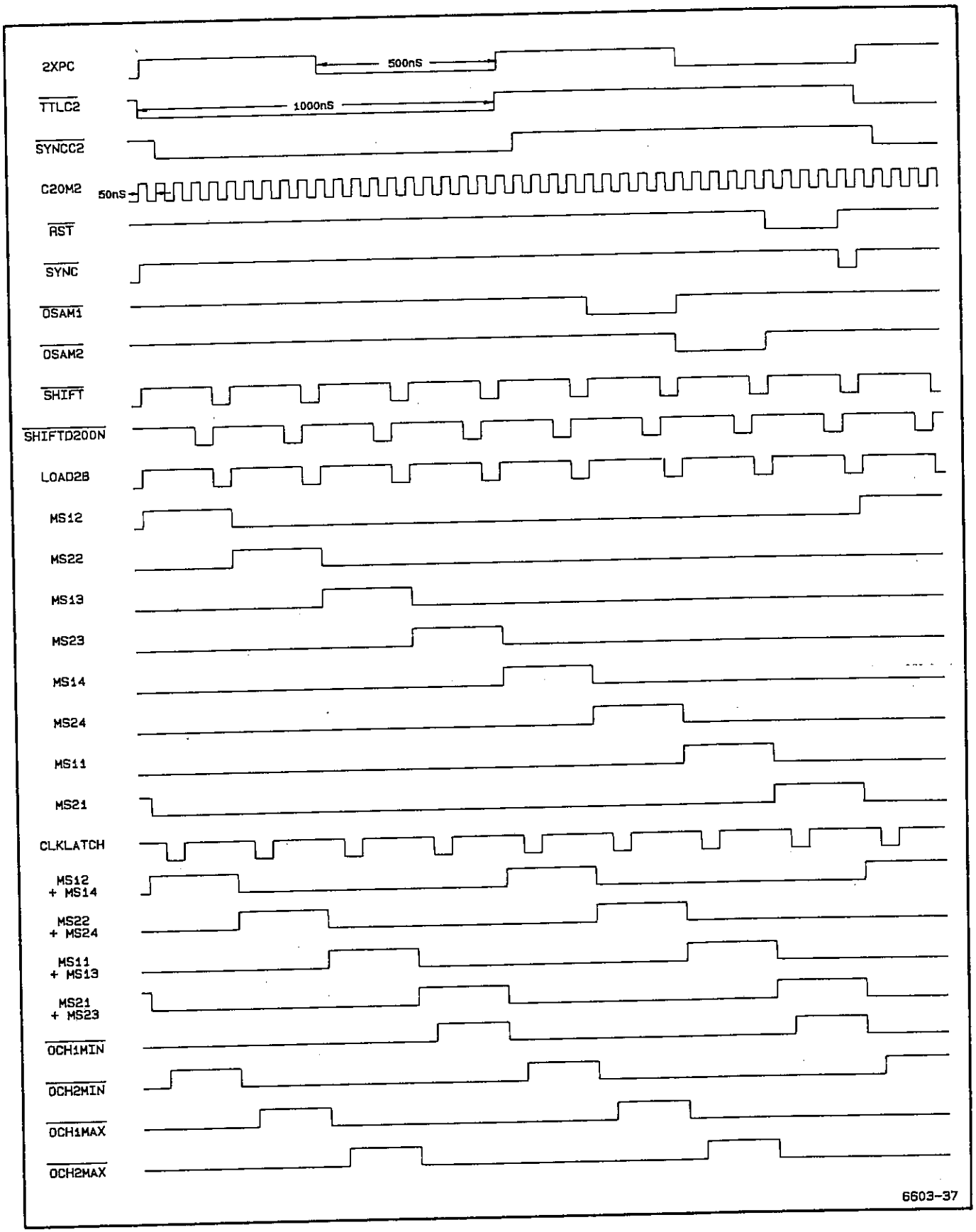


Figure 3-3. System Clock waveforms.

A similar 250 ns cycle occurs for the $\overline{OS2}$ LO state, ending with the LO being shifted to the Q_D output of U730. However, when the load is done to U621 this time, the $\overline{OS2}$ output to NAND-gate U620B is LO, and counter U621 is loaded with 0101 binary (the D_A) input from U620B is HI).

Since U621 now needs one less clock to count to 0111, $\overline{RST}$ (and thus $\overline{RESET}$ remains LO for 200 ns (rather than 250 ns as for $\overline{OS1}$ and $\overline{OS2}$), after which time the next load of U621 will occur. At the end of the reset time, both $\overline{RST}$ and the DA output of U620B are both LO, so counter U621 loads to 0000 binary. On the same 20 MHz clock, the LO $\overline{RST}$ level present on the SR data input of U830 is shifted right to the QA ($\overline{SYNC}$) output. This state (with $\overline{SYNC}$ LO) lasts one clock cycle (50 ns) only, because Q_C is still LO, causing LOAD to go HI and, therefore, causing the shift register to again shift right, resulting in SYNC going HI. On the next 20 MHz clock pulse, the $\overline{TTL2C}$ input is LO, causing $\overline{SYNC2C}$ to go LO on the clock edge. This starts the whole process over, and it is repeated until all samples have been moved out of the CCD arrays.

AND-gates U731A, U731B, and U731C buffer the outputs of counter U730 and ensure that the counter and the clock circuit will keep running even if a short occurs on the buffered $\overline{OSAM1}$, $\overline{OSAM2}$, or $\overline{RESET}$ lines.

CCD Data Clocks

The CCD Data Clocks (MS11, MS12, $\overline{MS13}$, $\overline{MS14}$, $\overline{MS21}$, MS22, MS23, and MS24) generated by counter U721, shift register U831 and U833, and the associated logic gating, are responsible for multiplexing the eight CCD array output levels (CH 1-1, CH 1-2, CH 1-3, CH 1-4, CH 2-1, CH 2-2, CH 2-3, and CH 2-4) onto the CCD DATA line for digitization by the A/D Converter. Figure 3-3 (shown previously) illustrates timing of the stage.

When the $\overline{SYNC}$ output from U830 pin 15 goes LO (for 50 ns at the end of the $\overline{TTL2C}$ cycle), the outputs of NAND-gate U620A and inverter U513D go HI, and the output of AND-gate U623A goes LO. This places counter U721 and shift registers U831 and U833 in their parallel load mode, and the next 20 MHz clock rising edge (start of next $\overline{TTL2C}$ loads in the fixed logic levels at their D inputs. The data bits (1000 binary) loaded into shift register U831 set the MS12 (multiplexer-select CH1 phase-2) output bit (pin 15) HI, with all other output bits LO. The LO $\overline{MS12}$ output from inverter U832D is applied to Q873 (diagram 14) to switch the CCD output data from the CH1 CCD array phase-2 output onto the CCD DATA line, where it is applied to A/D Converter U560 (diagram 15).

That same 20 MHz clock loads counter U721 with 1100 binary and clocks $\overline{SYNC}$ from pin 15 of U830 HI. With $\overline{SYNC}$ HI, shift register U831 is in hold mode, and counter U721 is enabled to count via AND-gate U623A. Counter U721 increments from the beginning count of 1100 to 0000 (four, 20 MHz clocks—200 ns), at which time the $\overline{SHIFT}$ output from OR-gate U522A goes LO. This sets up shift registers U831 and U833 (via U620A) to shift and, via U623A, places U721 in load mode. The next 20 MHz clock (at 250 ns) shifts a new LO from the SR data input of U831 into the Q_A output and shifts the HI from the Q_A output to the Q_B output (MS22). Counter U721 is also reloaded with 1100 binary for the next count cycle.

Similar 250 ns count cycles shift the HI bit to each output of shift registers U831 and U833 in succession until, during the last 50 ns of the HI state of the MS21 signal (U831 pin 15), $\overline{SYNC}$ goes LO again. The LO sets up U721, U831, and U833 to load on the next 20 MHz clock. The next clock (concurrent with $\overline{TTL2C}$ going LO) loads both U721, U831, and U833 and starts the cycle over again. The arrival of the $\overline{SYNC}$ signal ensures that the presetting load of U721, U831, and U833 always occurs concurrently with $\overline{TTL2C}$ going LO. The eight multiplexer-select clocks (and their inverted outputs) are thereby synchronized to CCD array output cycles.

The CCD Data Clock circuit also derives the signals used to multiplex the Acquisition Latch Switches. For Envelope mode acquisitions, these switches, in turn, select which byte of min/max data (stored in the Acquisition Latches) the Envelope Min/Max Comparator compares against a newly-acquired byte, A/D converted and output by the A/D Converter. (The Acquisition Latches and Acquisition Latch Switches, as well as the A/D Converter and Envelope Min/Max Comparator are found on diagram 15).

Briefly, the Acquisition Latch Switches need to "know" which CCD, CH 1's or CH 2's, and which CCD "side," minimum or maximum, is supplying the data byte being converted by the A/D Converter. MS11 and MS13, CH1 clocks, and MS21 and MS23, CH 2 clocks, are HI when a data byte from the minimum side of the CCD is being A/D converted; MS12 and MS14, CH 1 clocks, and MS22 and MS24, CH 2 clocks, are HI when a data byte from the maximum side is being converted. (Note that if the last digit of the clock name is odd, it clocks data from the minimum side of a CCD, and if it is even, from the maximum side. Also, note that the first digit indicates the CCD's channel. In other words, MS11 is Multiplexer-Select Clock CH 1, minimum side, MS22 is the Multiplexer-Select Clock for CH 2, maximum side, etc.) Gates U834A-D (diagram 7) logically OR these CCD Data Clocks to derive the multiplexing signals MS12+MS14, MS22+MS24,

MS13+MS11, and MS23+MS21 to drive these Acquisition Latch Switches. (For example, MS12+MS14 indicates that the data is from the minimum side of the CH 1 CCD and is HI if either MS12 OR MS14 is HI.) How these signals multiplex the Acquisition Latch Switches is explained in "A/D Converter and Acquisition Latches" in this section.

The CCD DATA Clock circuit supplies three other clocks used to properly time the transfer of A/D Converted CCD data: $\overline{\text{SHIFT}}$, derived as previously described, and CLKLATCH and $\overline{\text{SHIFTD200N}}$, derived from the $\overline{\text{SHIFT}}$ clock. $\overline{\text{SHIFT}}$ drives the shift-right input (pin 2) of shift-register U642, and C20M1 clocks the $\overline{\text{SHIFT}}$ clock successively through U642's outputs (QA-QD). Since C20M1 is the 20 MHz Clock and two 50 ns clock cycles are required before $\overline{\text{SHIFT}}$ appears at the QB output, CLKLATCH is delayed 100 ns from $\overline{\text{SHIFT}}$. Four clocks are required to clock $\overline{\text{SHIFT}}$ to the QD output, resulting in a 200 ns delay from $\overline{\text{SHIFT}}$ for $\overline{\text{SHIFTD200N}}$.

$\overline{\text{SHIFT}}$ clocks the A/D Converter, and CLKLATCH clocks the Acquisiton Latch Switches. The timing offset between the two clocks ensures the data byte output by the converter has stablized before it is latched into the Acquisition Latches. (The A/D Converter, Acquisition Latch Switches, and Acquisition Latches are found on diagram 15.) Similarly, $\overline{\text{SHIFTD200N}}$ is routed to NAND-gated U650B via inverter U835F (both found on diagram 8) for use in controlling the timing of the $\overline{\text{SAVEACQ}}$ signal to the Acquisition Memory. In this case, the time offset ensures that the data written from the Acquisition Latches to that memory has stabilized.

TIME BASE CONTROLLER AND ACQUISITION MEMORY

Time Base Controller (U670, diagram 8) and its associated gating circuitry generates the control signals and clocks to cause acquisitions in the various modes to occur. It keeps track of how the acquisition is progressing, starts the digitization of the samples by the A/D Converter when the correct number of data points have been acquired, and moves the digitized samples to Acquisition Memory (U600). The Acquisition Memory provides temporary storage of the converted data to permit the Waveform μP to access the data as it is needed to update the display.

Time Base Controller

Time Base Controller U670 monitors and controls the various acquisition functions. Two different operating modes of the CCD (charge-coupled devices) arrays must be controlled by U670; these are the FISO mode (fast-in, slow-out) and the Short-Pipe mode. FISO mode is used at sweep speeds faster than 100 μs/div when the analog sampling must occur at rates faster (1 MHz per channel and faster) than the maximum conversion rate of the A/D Converter. The Short-Pipe mode is used for lower frequency signals when the A/D conversion rate is much faster than the signals being sampled.

The major Time Base Controller functions in FISO (fast-in, slow-out) mode:

- Ensure that enough samples are in the CCD array "B" register to fill the "pretrigger" requirements.
- Ensure that the proper number of "post-trigger" samples are moved into the "B" register after triggering occurs.
- Discard the proper number of unneeded samples at the start of "slow-out" conversion.
- Ensure that exactly 1024 samples are moved to the Acquisition Memory during the "slow-out" conversion process.

Major functions in Short-Pipe mode:

- Ensure that valid data has made it through the "short-pipe" path of the CCD arrays.
- Synthesize the proper sample rate called for by the SEC/DIV setting.
- Ensure that enough samples have been saved in the Acquisition Memory to fill pretrigger requirements before enabling the Triggers.
- Ensure that the proper number of post-trigger samples are stored into the Acquisition Memory after the trigger event.

The instruction registers within Time Base Controller U670 are enabled when $\overline{\text{TBSEL}}$ from the System μP is LO. A register is selected for writing to or reading from by address lines A0, A1, and A2. Setup data from the System μP data bus is buffered to the selected register via bidirectional buffer U641 and written into the selected internal register by the $\overline{\text{WR}}$ (write) signal applied to pin 14. Acquisition mode, SEC/DIV setting, trigger position, and several other functions are controlled by the System μP via the commands written to the instruction registers within U670. Status data and register contents may be read out of the Time Base Controller registers by the System μP in a similar manner using the $\overline{\text{RD}}$ (read) signal to reverse the data paths in buffer U641 and the internal circuitry of U670.

The FISO (fast-in, slow-out, pin 36), ROLL (pin 2), and ENVL (envelope, pin 39) outputs are set indirectly by System μP writes to the internal control registers at the start of each acquisition cycle. Control signals are then output by an internal state machine of the Time Base Controller to dynamically control the acquisition circuitry in the required mode and signal acquisition rate (set by FISO). Writing to these "register" locations also allows the System μP to generate several strobes for internal latching and control functions.

A state machine internal to Time Base Controller U670 runs the acquisition process from start to finish. When all internal registers are properly loaded, the System μP writes to location 6022(h), generating a strobe that switches acquisition control to the Time Base Controller. This starts the acquisition system, and samples are taken in the defined mode. For FISO operations, the following occurs:

A counter internal to U670 begins counting $\overline{\text{TTLB1}}$ (TTL version of B clock—Phase 1) clocks to determine when at least enough samples have been transferred into the "B" register of the CCD arrays to fill "pretrigger" requirements. Samples will then continue to be placed in the B register, but no output samples will be saved until the record trigger occurs. (All 1088 locations in the four sides of 8 $\times$ 34 B register will fill if a record trigger does not occur before that many samples have been taken.) Each $\overline{\text{TTLB1}}$ clock represents 32 analog samples (four, 8-sample sides) transferred into the CCD array B register. When the proper number of pretrigger samples have been loaded, U670 will set its EPTHO (end of pretrigger holdoff) line HI. This signal enables Trigger Logic Array U370 (diagram 11), and the state machine in Time Base Controller U670 starts watching the SYNTRIG (synchronized trigger) input (pin 30) from the Phase Clock Array (U470, diagram 11) for the "record" trigger. In the meantime, the Trigger Logic Array will be counting delay clocks (DELCLK) to fulfill any specified delay requirements before a record trigger is permitted to be generated.

When the delay requirements are met, the SYNTRIG is allowed to occur when a trigger event occurs. The counter then watches $\overline{\text{TTLB1}}$ to determine when the proper number of post-trigger samples have been moved to the B register to meet the post-trigger requirements. Once post-trigger requirements are met, it sets SO (slow-out, pin 38) HI, which stops the sampling process and starts A/D conversion of the analog samples stored in the CCD array B register.

Since the trigger event can occur at any one of the 32 analog samples that are taken between each TTLB1B clock, and since the Time Base Controller only keeps track of the number of pretrigger and post-trigger samples in terms of these 34-sample records, there are usually some samples at the beginning of those in the CCD array B register that are extra. When the analog samples are serially moved out of the CCD array for digitization, these extra samples must be ignored in order to maintain proper trigger location within the complete record. The CCD Phase Clock Array (U470) knows where the record trigger occurred relative to the $\overline{\text{TTLB1}}$ pulse (1-of-32 position) and sends this information to U670 on the TL0-TL4 (trigger location bits 0 through 4) lines. This trigger-location number is loaded into the counter and, as the samples are moved out of the CCD array, that number of extra samples is essentially discarded. Those samples are A/D converted but will not be stored because U650B is not yet enabled to gate the $\overline{\text{SAVEACQ}}$ signal used to write the data into the Acquisition Memory.

Once the extra samples have been counted, the ACQUIRE output is set HI. In FISO mode, six more samples are counted out via shift register U750, enabling U650B. Since the instrument is in FISO mode, the output of U512C will be HI and the $\overline{\text{SAVEACQ}}$ signal that is used to save waveform data into the Acquisition Memory (via U501) is controlled by the output of U835F (SHIFTD200N). This input to NAND-gate U650B is a delayed version of the SHIFT (4 MHz) clock. The 200 ns delay provided ensures that the A/D Converter output byte has settled before being written to the Acquisition Memory.

When the Time Base Controller is in control of writing data to the Acquisition Memory, the $\overline{\text{SAVEACQ}}$ clock is routed through U501 of the Mode Control Logic and becomes the $\overline{\text{WE}}$ (write enable) clock used to write waveform data into Acquisition Memory U600. That data is obtained from the Acquisition Latches (diagram 15) via buffer U613. The $\overline{\text{WE}}$ signal is also used to increment the Memory Address Counter (U300, U400, and U401), the result being that digitized samples from the Acquisition Latches are saved interleaved in consecutive memory locations. Each address is latched into the Record-Start Address Latches (U502 and U601) as the data-write ends, so that the address of the last-stored sample is always available. This information is used as a pointer when generating waveform displays.

As the digitized samples are moved to Acquisition Memory, an internal counter in Time Base Controller U670 watches the MS23+MS21 and MS22+MS24 clocks (pins 6 and 28) to determine when 1024 points (or 512 max/min pairs in Envelope mode) from each CCD array (CH 1 and CH 2) have been stored. When 2048 samples have been saved, the Time Base Controller will set ACQUIRE (pin 24) LO, disabling memory saves, and it will set its ACQDN (acquisition done) status line (pin 25) HI. The Waveform μP (U470, diagram 2) then takes over for transfer of the acquired waveforms to the Waveform μP Save Memory.

When the Waveform μP (U470, diagram 2) reads the HI ACQDN status via U542 (diagram 2), it reads the address

of the last-saved point from the Record-End Latch (U502 and U601). Since the Acquisition Memory addresses are circular (incrementing the Address Counter from its last address goes back to the first address), it knows the record begins at the next address. With TB2MEM LO, the $\overline{ACQ}$ signal is routed through Mode Logic Switch U501 to become the $\overline{WP2MEM}$ signal. The $\overline{ACQ}$ signal going LO from the Waveform μP via address decoder U570 enables data buffer U610 to permit the Waveform μP to access the waveform data stored in the Acquisition Memory (see "Waveform Processor System" description).

SHORT-PIPE OPERATION. Short-Pipe operation is similar to FISO in the way mode and setup data is loaded and the way the internal counter is used to keep track of various events. The major differences are: Short-Pipe mode moves input samples directly from the CCD array "A" register input, down the first "B " register channel and out of the CCD array through the "C" register. Short-Pipe mode must also synthesize the sample clock rate.

To synthesize the sample rate for the Short-Pipe mode, FISO (from U670 pin 36) is set LO by the System μP, thereby enabling the CE2B/N (clock enable 2B divided by N) input to U512C. The CE2B/N clock (along with the SHIFTD200N clock) then controls saving the waveform data into the Acquisition Memory. In Short-Pipe mode, CCD sampling occurs at a continuous 2 MHz rate, but due to SEC/DIV setting data written to an internal counter in U670, the synthesized $\overline{CE2B/N}$ clock will only allow every "Nth" point to be saved in Acquisition memory to produce only 50 data points per division in the display. Samples between the saved Nth points are ignored. The synthesized $\overline{CE2B/N}$ clock will only enable U650B long enough to save either two or four points and is dependent on the sweep-rate division factor written to the internal counter. This allows effective sample rates down to 1 sample every 2 μs (100 μs/div) to be achieved. The 2XSDC (two-times-slow-delay clock, U670—pin 29) runs at half of this effective sample rate. This 2XSDC clock divided by two at the Q output of U720B and buffered by U680C to produce SDC. SDC allows the Trigger Array to count one delay period per every four sample intervals.

Since CCD array samples are moved directly from the input to the output via the first B register and since stored samples may occur at a rate different than the sample rate, pretrigger and post-trigger counting is done relative to samples actually stored into the Acquisition Memory. When enough valid pretrigger points have been saved, EPTHO enables the Triggers. Data is saved in bursts of two points (four points in ENVELOPE acquisition mode), one for CH 1 and one for CH 2, at the synthesized rate. When the trigger event occurs, U670 counts the proper number of post-trigger samples. When the post-trigger count is complete, since A/D converted data already is stored in Acquisition Memory, ACQDN is set. Waveform data bytes are moved to the Save Memory by the Waveform μP and control is given back to the System μP.

LOAD LATCHES FLIP-FLOP. In Envelope Mode, Load Latches flip-flop U651A puts out a signal at the beginning of each envelope sampling interval that is HI for four acquisition cycles. That HI LOAD LATCHES signal loads the first eight acquired data points (four min-max pairs) into the Acquisition Latches to be used for min-max comparison to the following waveform samples in that Envelope sampling interval.

The Set input of U651A is HI during Envelope, the output of the flip-flop is controlled by the MS23 clock and the CE2B/N clock (on the D input). The CE2B/N clock is a divided down MS22 clock, with the division factor depending on the SEC/DIV setting. The division factor determines how many waveform samples will be compared for new max and new min data during each envelope sampling interval. Only the maximum and minimum waveform data point values that occur during the envelope sampling interval are transferred to the Acquisition Memory.

For non-envelope acquisitions, ENVL is LO. The Set input of flip-flop U651A is therefore asserted, and U651A will be held in the Set state with the Q output (LOAD LATCHES) held HI. That constant HI signal applied to the Acquisition Latch Switching circuitry causes each data point acquired to be loaded into the Acquisition Latches and transferred into Acquisition Memory.

ROLL LOGIC. In ROLL mode the display is constantly being updated as new data points are available. A means is provided to tell the Waveform μP when new data points are available. An interrupt to the Waveform μP is generated by the Roll Logic flip-flop, U651B. When the ACQUIRE signal from Time Base Controller U670 goes HI, new waveform data points are acquired. The HI state of that signal is clocked to the Q output of flip-flop U651B on the rising edge of the $\overline{CE2B/N}$ signal; the same signal that causes the sample data to be saved into the Acquisition Memory in Short-Pipe mode. The PTAVAIL signal at the Q output is an interrupt to the Waveform μP. When the Waveform μP services the interrupt request, it sets $\overline{PTACK}$ (point acknowledge) LO via U500B and U500C to reset the flip-flop in preparation for the next new data points. The saved points are also moved to the Save Memory and then to the Display Memory for a display update.

In NORMAL mode, the ROLL signal is LO, and NAND-gate U500B outputs a continuous logic HI that holds the Roll Logic flip-flop in the Reset state (with the Q output LO).

Memory Mode Control

The Memory Mode Control circuit is made up primarily of Mode Selector Switch U501, a quad 2-to-1 multiplexer that switches control signals between those of Time Base Controller U670 and those of the Waveform μP. Selection is done by the TB2MEM signal from AND-gate U731D pin 11.

The $\overline{WE}$ (write enable) output from Mode Selector Switch U501, pin 12, controls both writing into the Acquisition Memory and incrementing of the Address Counter. With TB2MEM set LO, the $\overline{WWR}$ (Waveform μP write) signal gated through OR-gate U512D to the 4A input (pin 13) of U501 controls writing to the Acquisition Memory. The $\overline{OE}$ (output enable) derived from the Waveform μP $\overline{WRD}$ (Waveform μP read signal), controls the output of Acquisition Memory data. It is asserted LO only when the Waveform μP is trying to read Acquisition Memory locations.

With TB2MEM HI, the $\overline{SAVEACQ}$ signal from NAND-gate U650B, is selected as the $\overline{WE}$ signal, and the $\overline{OE}$ is set HI to disable the Acquisition Memory from outputting data. Data buffer U613 is enabled by the LO level of the $\overline{EOE}$ signal from pin 7 of the Mode Select Switch to connect the Envelope Logic Latch bus to the input bus of the Acquisition Memory.

When the Waveform μP wants to access the Acquisition Memory, it will set the $\overline{ACQ}$ line LO to enable its control signals to the inputs of Mode Logic Switch U501 and wait for the delayed ACQUIRE signal from U750 (diagram 8) to go LO (indicating that the Time Base Controller is finished acquiring). When the delayed ACQUIRE goes LO, the output of AND-gate U731D (TB2MEM) goes LO and the Mode Logic Switch select the Waveform μP signals to control the Acquisition Memory. The LO TB2MEM signal also sets the Address Counters to their Load state, and the counter outputs then follow the WA0-WAA (Waveform μP address bits 0-A) lines, giving direct access to Acquisition Memory data locations by the Waveform μP.

Address Counter

The Address Counter increments the Acquisition Memory address as each point is saved. Each write into Acquisition Memory ends with the $\overline{WE}$ (write enable) signal going HI, clocking the counter to address the next sequential Acquisition Memory location.

The TB2MEM signal from AND-gate U731D controls the mode of the Acquisition Memory Address Counter (composed of binary counters U300, U400, and U401). When the TB2MEM signal goes LO, the counters become "transparent." This connects the Waveform μP address bus to the address inputs of the Acquisition Memory so that the Address Counter output follows the WA0-WAA (Waveform μP address bits 0-A) lines. When the TB2MEM signal is HI, the Time Base Controller is in control of the Acquisition Memory, and counter will be in its count mode as the acquired signals are being stored into the Acquisition Memory.

Acquisition Memory

Acquisition Memory U600 is a random-access memory device (RAM) that provides temporary storage of acquired data points before they are moved into Save Memory. Analog waveform samples from the CH 1 and CH 2 CCD arrays are digitized and moved into Acquisition Memory under control of the Time Base Controller (diagram 8), alternating CH 1 data with CH 2 data. The Waveform μP reads the data out of Acquisition Memory via buffer U610, unscrambles it, and moves it to proper Save Memory locations.

MEMORY INPUT BUFFER. Memory Input Buffer U613 applies the time-multiplexed waveform data bytes from the Acquisition Latches (diagram 15) to the data inputs of the Acquisition Memory inputs at all times except when the Waveform μP is accessing the Memory. Inverter U620D inverts the most-significant bit of the sample data so that range center of the A/D Converter output corresponds to 00 hex (center screen value), thereby creating bipolar data referenced to center screen.

Record-End Latch

The Record End Latch composed of U502 and U601 continually latches the address of the last Acquisition memory location that was written. The latch is clocked on the rising edge of the $\overline{WE}$ clock (from the $\overline{SAVEACQ}$ signal or the Waveform μP $\overline{WWR}$ signal via Mode Logic Switch U501) and provides the Waveform μP with the last address written (the end of the record for a full acquisition) by the Time Base Controller or read by the Waveform μP. Since the Acquisition Memory addresses are circular, the start of a FISO record will always be the Record End address plus one. In Short-Pipe mode, the Waveform μP will read those (two for normal, four for envelope) points immediately preceding (and including) the Record End address. The latched address (plus the trigger location data) is placed on the Waveform μP data bus by asserting $\overline{RDMAR0}$ and $\overline{RDMAR1}$ (read memory address) lines.

Two-to-one multiplexer U722B applies either trigger-location bit 4 (TL4) or the Time Base Controller TBTRIG (time base triggered) status bit to latch U502, depending

on whether FISO or Short-Pipe mode is called for. The TBTRIG bit used in Short-Pipe mode tells the Waveform μP when the Time Base Controller detected Record Triggering.

ATTENUATORS AND PREAMPLIFIERS

The Attenuator and Preamplifier circuitry (diagram 9) allows the operator to select the vertical deflection factors. The Front Panel μP monitors the Channel VOLTS/DIV switches and VOLTS/DIV VAR controls and passes changes to the settings to the System μP which then digitally switches the attenuators and sets the Preamplifier gains accordingly. Vertical Couplings are similarly controlled.

Channel 1 and Channel 2 Attenuators

The Channel 1 and Channel 2 Attenuators are identical in operation, with corresponding circuitry in each channel performing the same function. Therefore, only the Channel 1 circuitry is described.

An input signal from the Channel 1 input connector is routed through an attenuator network by four pairs of magnetic-latch relay contacts. The position of the relays is set by data placed into Attenuator Control Register U511 by the System μP. Relay buffers U510 and U520A and ATTEN CLK circuitry, U520D, Q620, and Q621 provide the necessary drive current to the relay coils.

Four input coupling modes (1 MΩ AC, GND, 1 MΩ DC, and 50 Ω DC) and three attenuation factors (1X, 10X, and 100X) may be selected by closing different combinations of relay contacts. The relay contacts are magnetically latched and, once set, remain in position until new attenuator settings are loaded into the Attenuator Control Register and clocked by the ATTEN CLK circuitry. (See the "Attenuator Control Register" description for a discussion of the relay-latching procedure.) The three attenuation factors, along with the programmable and variable gain factors of the Vertical Preamplifier, are used to obtain complete range of vertical deflection factors.

The 50 Ω termination resistor has a thermal sensor associated with it that produces a dc voltage (CH 1 OVL) proportional to the input power. Should the input power exceed the normal safe operating level for the 50 Ω DC input, the output voltage from the thermal sensor will exceed the normal operating limit. The amplitude of this dc level is periodically checked by the Front Panel μP to detect if an overload condition is present. If an overload occurs, the System μP switches the input coupling to the 1 MΩ position to prevent damage to the attenuator, and the error message "50 Ω OVERLOAD" is displayed on the CRT. At power-off, the input coupling is automatically switched to the 1 MΩ position to prevent an unmonitored overload condition from accidently occurring.

Compensating capacitor C414 is manually adjusted at the time of calibration to normalize input capacitance of the preamplifier to the attenuator.

A probe-coding ring around the BNC input connector passes probe-coding information (a resistance value to ground) to the Front Panel μP for detection of probe attenuation factors. The readout scale factors are then set to reflect the attenuation factor of the attached probe.

Attenuator Control Register and Attenuator Clock

The Attenuator Control Register, composed of shift registers U511 and U221, allows the System μP to control the settings of the input coupling and attenuation factors. To set the input coupling mode and attenuation factors for Channel 1 and Channel 2, a series of eight 16-bit control words is serially clocked into U221 and U511 (eight bits in each register). Each control word is used to set the position of one of the eight attenuator and coupling relays (four relays are in each attenuator assembly). Each control word will have only the bit corresponding to the specific relay contact to be closed set HI. Relay buffers U510 and U520A (for Channel 1) and U220 and U520B (for Channel 2) are open-collector drivers that invert the polarities of all bits. This results in a LO being applied to only the coil lead associated with the contact to be closed; all other coil leads are held HI.

ATTENUATOR CLK CIRCUIT. To set a relay once the control word is loaded, the System μP generates an ATTN CLK (attenuator clock) to U520D pin 4 via R530 and C530. The strobe pulses the output of U520D LO for a short time. This output pulse attempts to turn on both Q620 and Q621 (relay drivers) via their identical base-bias networks. Due to the lower level from the turned on Darlington relay buffer (coupled through the associated coil diode and either CR610 or CR622 to one of the bias networks), one transistor will turn on harder as the ATTN CLK pulse begins to forward bias the transistors. The more positive collector voltage of the transistor turning on harder is fed through the bias diode (again either CR610 or CR622) to further turn off the opposite transistor. This action results in one transistor being fully on and the other one being fully off. The saturated transistor supplies a current path through the two stacked relay coils to the LO output of either U221 or U511 to close the selected contacts. Once set, the magnetic-latch feature will hold the relay set to this position until opposing data is clocked into

the Attenuator Control Register and strobed into the relay. All coil leads for the remaining relays are set HI, and only the selected relay will be set.

To set the seven remaining Attenuator and coupling relays, the sequence just described is repeated seven more times. Whenever the System μP is informed by the Front Panel μP that the attenuation factor or input coupling has changed, the entire relay-setting procedure is repeated for all eight relays.

The MSB (most-significant bit) of the Attenuator Control Register, ATD15, is routed back to the System μP via CR287 and U380A (diagram 5), allowing diagnostic readback of the register contents.

Channel 1 Preamplifier

Preamplifier U420 converts the single-ended input signal from the Channel 1 Attenuator to a differential output signal used to drive the Channel 1 Peak Detector (U440, diagram 10). The device provides amplification in predefined increments, depending on the control data written to it from the System μP. The Preamplifier also has provisions for signal inversion, variable gain, vertical %positioning, trigger signal pickoff, and balance control.

The Channel 1 vertical input signal is applied to pin A of Channel 1 Preamplifier U420 via C1005 and R1005. The two series diodes to the −8 V supply, CR410 and CR411, protect the Preamplifier input from excessive negative voltages. The differential Preamplifier signal outputs (+OUT and −OUT) sink 12 mA of common-mode current from the Channel 1 Peak Detector inputs and drive those 75 Ω inputs with a 0.25 mA per division output signal.

Control data from the System μP is clocked into the internal control register of U420 via pin 22 (CD) by the clock signal applied to pin 23 (CC). This data causes the Preamplifier either to multiply the normalized gain (5 mV/div) by 2.5 or 1 or to divide the normalized gain by 2, 4, or 10. The resulting sensitivities are 2 mV/div, 5 mV/div, 10 mV/div, 20 mV/div, and 50 mV/div respectively.

Four analog control voltages set by the DAC System circuitry (diagrams 5 and 6) modify the differential output signal at pins 9 and 10 of the Preamplifier. CH1-BAL (Channel 1 Balance) is applied to U420 pin 2 from the sample-and-hold circuit formed by U641B and C648 (diagram 5). This signal is a dc-offset level determined during the auto-calibration procedure. The offset value is stored as a calibration constant in nonvolatile memory and, like the other DAC System outputs, is updated approximately every 64 ms, holding the Preamplifier in a dc-balanced condition.

The voltage level of the CH1-PA-POS (Channel 1 Preamplifier Position) signal, from the circuit which includes U630A and U630B (diagram 6), vertically positions the channel 1 trace. When the CH1 VERT POS control on the Front Panel is turned, the Front Panel μP detects the change and reports it to the System μP. The System μP incorporates the change and causes subsequent DAC System updates to reflect the new value in the analog voltage level of the CH1-PA-POS signal.

A user may change the Channel 1 variable gain by pressing the CH1 VARIABLE button and pressing the appropriate menu choice buttons. The Front Panel μP detects these switch closures and reports them to the System μP. The System μP modifies the memory value that is sent to the DAC System to reflect the user-defined variable gain factor in the CH1-GAIN-CAL signal. The memory value that is modified is the calibrated value derived at the time of instrument self-calibration and stored in nonvolatile memory. Selecting the CAL menu choice removes the variable gain modification and returns the calibrated gain setting.

The TRANADJ1 control voltage, applied to U420 pin 6 from U661D (diagram 6), compensates for the variation in Preamplifier high-frequency response that occurs when the preamplifier gain setting is varied. Appropriate control voltages for each gain setting are determined at factory instrument calibration and stored in nonvolatile memory as calibration constants. They are modified only at instrument calibration times.

The network of R525, L460, variable C456, and variable R436 provide additional adjustment of the overall frequency response of the system.

A pickoff amplifier internal to U420 conditions the trigger signal and provides the proper signal level at pin 15 to drive the A/B Trigger Generator (U150, diagram 11). The pickoff point for the trigger signal is prior to the addition of the vertical-position offset, so the position of the signal on the CRT has no effect on the trigger operation. However, the pickoff point is after the Preamplifier balance and variable gain have been added to the signal, so both of these functions affect trigger operation.

Common-mode signals are rejected from the trigger signal by the circuitry composed of operational amplifier U230B and associated components. The inverting input of U230B (pin 6) is connected to the common-mode point

between +PICK (pin 12) and −PICK (pin 15) of U420. Any common-mode signals present are inverted and applied to a common-mode point between R133 and R235 to cancel the signals from the differential output. A filter network composed of LR421 and a built-in circuit board capacitor reduces trigger noise susceptibility.

The drain voltage for the input FET of the Preamplifier is provided by the circuit composed of VR420, R512, R515, and R516. Resistors R516 and R515 are part of the self-calibration circuitry and are used to match the gain of the CH1-BAL signal (pin 2) with that of the output of the attenuator.

Channel 2 Preamplifier

Operation of Channel 2 Preamplifier U320 is nearly identical to that of the Channel 1 Preamplifier just described. The exceptions are that the signal obtained from the pickoff reverse-termination return (pin 11) is used to drive the rear-panel CH 2 OUT connector and that the signal from the positive trigger pickoff (pin 12) is used to drive the Video Option Back-Porch Clamp circuit (diagram 21). The output of that clamp circuit is an offset signal, applied to the Channel 2 Preamplifier at pin 3, that is used to remove ac power-supply hum from the display of a video signal applied to the Channel 2 input when the Video option is in use.

The amplified Channel 2 +PRTR signal from U320 pin 11 provides an accurate representation of the Channel 2 signal at the rear-panel CH 2 OUT connector. The +PRTR pickoff signal is applied to the emitter of Q240B via a voltage divider formed by R234, R241, and R240. Transistor Q240B, configured as a diode, provides thermal compensation for the bias voltage of Q240A and reduces dc level shifts with varying temperature. Emitter-follower Q240A provides the drive and impedance matching to the CH 2 OUT connector and removes the diode drop added by Q240B. Clamp diodes CR140 and CR141 protect Q240A should a drive signal be accidentally applied to the CH 2 OUT connector.

External Trigger Preamplifier

The functions provided by External Trigger Preamplifier U100 are similar to those provided by the Channel 1 and Channel 2 Preamplifiers. The single-ended EXT TRIG 1 and EXT TRIG 2 input signals are buffered by U100 and routed to A/B Trigger Generator U150 (diagram 11) where they are available for selection as the trigger source for either the A or B trigger signal.

External trigger signal sensitivities may be set by the user to allow triggering ranges of either ±0.9 volts (EXT ÷ 1) or ±4.5 volts (EXT ÷ 5). Larger applied voltages on the external trigger inputs will exceed the control ranges of the Trigger System. The logic levels of control bits applied to U100 pin 30 (GA3) and pin 31 (GA4) from Source Select Control Register U140 (diagram 5) set the gain of the EXT 1 and EXT 2 Preamplifiers respectively.

Dc offsets in the output signal due to any tracking differences between the +5 V and the −5 V supply to U100 are reduced by the Tracking-Regulator circuit composed of U120, Q110, and associated components. Operational amplifier U120 and Q110 is configured so that the output voltage at the emitter of Q110 follows the −5 V supply applied to R210. This tracking arrangement ensures that the supply voltages are of equal magnitude to minimize dc offsets in the output signals.

PEAK DETECTORS AND CCD/CLOCK DRIVERS

The Peak Detectors and CCD/Clock Driver arrays (diagram 10) form what is essentially a very fast analog shift register. Waveform samples from each Preamplifier (U320 and U420, diagram 9) are loaded into the shift register array at a selected sample rate up to 500 Megasamples per second and clocked out of the array at a slower, fixed rate for digitization by the A/D Converter (see diagram 15).

Peak Detectors U340 and U440 are hybrid devices having two modes of operation: "track" and "peak detect." For NORMAL and AVG (average) acquisition modes, the Peak Detectors track the input signal and provide signal gain from the Preamplifiers to the CCD arrays. In the peak-detect mode used for ENVELOPE acquisitions at sweep speeds of 500 ns per division and slower, the Peak Detectors detect and hold the most positive and the most negative amplitude value of the input signal that occurs during each sampling interval. The peak values are amplified as in the NORMAL and AVG modes and applied to the input registers of the CCD arrays to produce a composite waveform of the most positive and most negative waveform amplitudes.

CCD/Clock Drivers U350 and U450 are hybrid devices containing a charge-coupled device (CCD) integrated circuit, a Clock Driver integrated circuit, and a symmetry-delay adjustment integrated circuit. The charge-coupled devices are very fast analog shift registers. Differential signals applied to the inputs of the CCD's from the Peak Detectors are sequentially clocked into the CCD registers at the processor-selected sample rate as determined by the SEC/DIV switch setting. Movement of the analog samples through the CCD arrays is controlled by the Clock Driver circuitry of the devices. Shifting the samples out of the CCD to be digitized is done with the combined clocking action of the internal Clock Drivers and the clock signals

supplied externally to the CCD via Q450, Q460, and Q551. All control logic for the CCD/Clock Drivers, with the exception of the $\overline{\text{RESET}}$ signal from the System Clock circuitry (diagram 7), is derived from Phase Clock Array U470 (diagram 11).

Signal samples from both vertical channels are continuously loaded into and shifted through the CCD arrays until a trigger event occurs. The Time Base Controller (U670, diagram 8) then allows a specific number of further analog samples to be shifted into the arrays depending on the number of post-trigger samples needed to fill the waveform record. That number is determined by the TRIG POSITION setting for the acquisition. When the necessary samples have been loaded into the arrays, sampling is halted. The differential analog samples stored in the CCD arrays are then shifted out of the CCD to the CCD Output circuitry (diagram 14) where they are conditioned and multiplexed to the A/D Converter to be digitized.

Peak Detectors

The Peak Detectors provide peak detection, gain, and buffering of the CH 1 and CH 2 signals. Peak detection is enabled for ENVELOPE mode acquisitions, and then only when the acquisition rate is 500 ns per division and slower, but signal buffering is provided for all acquisition modes. Operation of both Peak Detectors is the same; therefore, the description is limited to the CH 1 circuitry. A simplified block diagram of the Peak Detector is shown in Figure 3-4.

Two user-selectable bandwidth limiters provide bandwidth reductions to either 20 MHz or 100 MHz for the signal through the Peak Detectors. With the Video Option installed, one of the 20 MHz limiter coils (L531 for CH 1) is adjustable to optimize the 20 MHz response for video signal operation. Without the option, both 20 MHz bandwidth limit coils for each Peak Detector are fixed values. The 100-MHz bandwidth is adjusted by R431 for CH 1. The input stage of the Peak Detector is where bandwidth limiting is switched. Three bandwidth-select bits (FULL, 100MHZ, and 20MHZ) applied from the Peak Detector Control register (U530, diagram 5) control the bandwidth. Only one control bit at a time is set HI, and that bit controls the input amplifier bandwidth accordingly.

The differential signal from the CH 1 Preamplifier is applied to the CH 1 Peak Detector (U440) on input pins 4 and 6. In ENVELOPE acquisition mode, two sets of two fast-peak detectors following the input stage are used to permit continuous peak detection of negative and positive peaks of the input signal. While the PDA fast-peak detector is detecting a negative peak, the PDB peak detector is holding the last peak or resetting and vice versa (see table in Figure 3-4). Each of fast-peak detectors is followed by a slow-peak detector to increase the peak-hold time to the CCD input register. The outputs of the positive peak detectors are multiplexed to the differential OUTEVEN pins (pins 33 and 35) while the outputs of the negative peak detectors are multiplexed to the differential OUTODD pins (pins 26 and 28).

For NORMAL and AVERAGE acquisition modes, the Peak Detector operates in the track mode. To track the input signal and supply buffering only to the input signal, pin 21 (PD) is set HI and pin 22 (SLOW/FAST is set LO, and the differential peak-detector clock signals (PD1 and PD2) are held at fixed levels (PD1 LO and PD2 HI). The signals bypass the internal peak detector stages and proceed directly to the output stages. The differential outputs at OUTODD and OUTEVEN follow the input signal at a signal level of 200 mV/division. Loading of the outputs is provided by resistor networks inside the CCD/Clock Driver which return to adjustable voltage sources VCC13 and VCC24 provided by the Common-Mode Adjust circuits (discussed later).

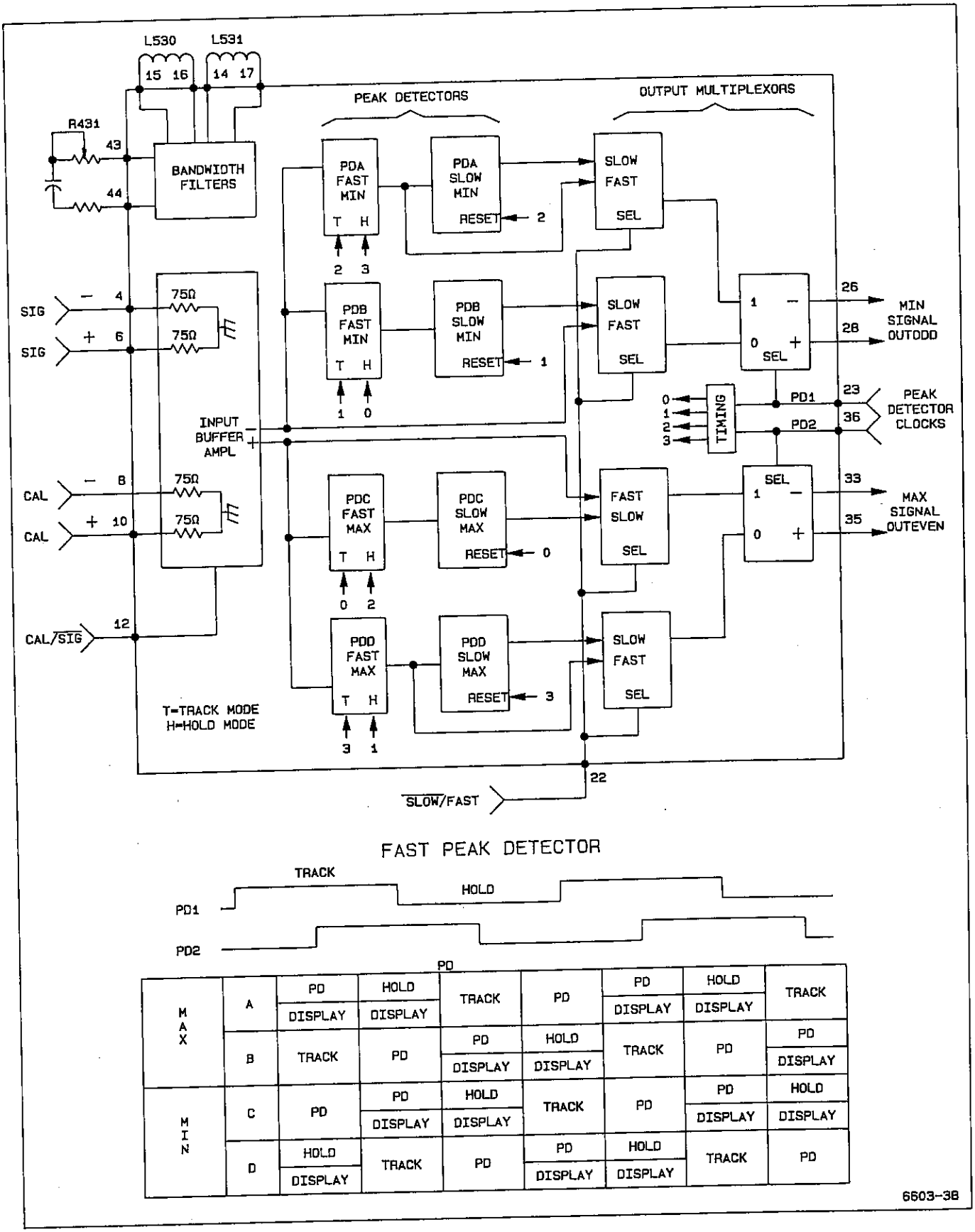
Peak detect mode for ENVELOPE acquisitions is turned on by setting $\overline{\text{PD}}$ LO at pin 21 and SLOW/FAST HI at pin 22 of Peak Detector U440. The differential ECL peak-detector clock signals (PD1 and PD2) toggle under control of the Phase Clock Array (U470, diagram 11) to control the internal peak detector switching and multiplexing of the positive and negative peaks to the OUTODD and OUTEVEN stages. The table in Figure 3-4 shows timing of the peak detector clocks and illustrates how alternate peaks are applied to the IN13 and IN24 inputs of the CCD.

Bias current for the input stage of U440 is set by R430 on pin 47, and output stage bias is set by R440 on pin 32.

The +CAL and −CAL inputs at pins 8 and 10 are identical to the signal inputs, but they are used only for the application of test signals during calibration or diagnostic testing. Selection of the inputs is controlled by the CAL/SIG signal. The test signals applied to pins 8 and 10 from the DAC System are used for testing and calibrating the Peak Detectors, the CCD/Clock Drivers, the CCD Output circuits, and the A/D Converter.

Common-Mode Adjust

The Common-Mode Adjust circuits (U540A and B, Q540, Q640, and associated components) vary, under control of the System μP, the common-mode voltage levels at the output of the CH 1 Peak Detector. (Similar circuitry performs the same task for the CH 2 Peak Detector.) These voltages are adjusted at instrument calibration to optimize CCD operation. The CH 1-OUTODD Common-Mode Adjust circuit is described; the remaining Common-Mode Adjust circuits operate identically.



FAST PEAK DETECTOR

		PD						
MAX	A	PD DISPLAY	HOLD DISPLAY	TRACK	PD	PD DISPLAY	HOLD DISPLAY	TRACK
	B	TRACK	PD	PD DISPLAY	HOLD DISPLAY	TRACK	PD	PD DISPLAY
MIN	C	PD	PD DISPLAY	HOLD DISPLAY	TRACK	PD	PD DISPLAY	HOLD DISPLAY
	D	HOLD DISPLAY	TRACK	PD	PD DISPLAY	HOLD DISPLAY	TRACK	PD

6603-38

Figure 3-4. Simplified Peak Detector block diagram.

U540A, Q640, and associated circuitry are configured as an operational amplifier capable of high current output. This "op-amp" outputs a supply voltage as VCCODD to the Peak Detector, U440, and as VCC13 to the CCD/Clock Driver, U450. It compares VCCODD/VCC13 with the CM10DD control voltage suplied by the DAC system and varies VCCODD/VCC13 dependent on control voltage. Varying VCCODD/VCC13 controls the common-mode voltage levels at the peak detector outputs which, in turn, optimizes the CCD operation.

The op-amp configuration sources both the load current for the OUTODD Peak Detector's differential output stages, OUTODD+ and OUTODD−, as well as the VCCODD voltage supply to those output stages. Outputs OUTODD+ and OUTODD− always sink a common-mode current of 45 mA. This constant current, sourced by R651 and Q640 of the op-amp, flows through internal load resistors inside the CCD/Clock Driver, U450. Since these resistors provide a common-mode load of 50 Ω, a constant 2.25 volts is dropped from the VCC13 source at pin 13 to the differential inputs IN13+ and IN13− at pins 11 and 12 of the CCD/Clock Driver.

If the CM10DD voltage set is changed by the System μP, operational amplifier U540A compares the VCCODD level with the attenuated CM1ODD level output from the DAC System. The output of U540A drives Q640 to supply more or less current to its collector circuit. The constant 45 mA common-mode current drawn by pin 13 of U450 doesn't change; therefore, the change in current serves to raise or lower the supply voltage to the peak detector output stages at pin 25 of U440.

R651 reduces stress on Q640 by supplying part of the total current sourced to the peak detector outputs, via pin 13, U450, and the Voltage supply for those stages, via pin 24, U440. Emitter resistor R647 current-limit protects Q640 if a short or overload occurs. Resistors R647 and R651 also limit the voltage gain of Q640 to stabilize the feedback loop of the Common-Mode Adjust circuit.

Charge-Coupled Devices (CCD)

The CCD portion of the CCD/Clock Driver hybrid is a MOS-type integrated circuit that functions as a very fast analog shift register. A signal applied to the input is sampled by being converted to charge packets. These charge packets are then shifted through the CCD registers by MOS-circuit gating at intervals determined by the clock rates applied by the Clock Driver integrated circuit portion of the hybrid. The internal arrangement of the CCD analog shift registers and the total amount of storage space permits the input signal to be sampled at a high clock rate when necessary for the higher frequency signals. The charge packet samples are temporarily stored and then shifted out of the CCD at a much slower rate than the sampling rate. An inexpensive A/D Converter can be used to digitize the signal and slower memory circuits used to store the digitized samples. This type of operation is called Fast-In-Slow-Out (FISO) and is used at SEC/DIV settings of 50 μs and faster. At SEC/DIV settings of 100 μs and slower, the CCD runs with a constant clock rate of 500 kHz in a mode called Short Pipeline (discussed later).

A simplified diagram of one-quarter of one CCD is shown in Figure 3-5. The quarter shown, called Side 1, is nearly identical to the other three sides (2, 3, and 4) of the CCD. Although all four sides of a CCD shift charge packets simultaneously, they take samples 90 degrees out-of-phase with each other, thereby achieving an effective sample rate of 500 Megasamples per second while clocking each CCD side at only an 8 ns rate.

Each of the four sides of each CCD can temporarily store 272 analog samples for a total of 1088 samples per channel. Although only 1024 samples are needed for conversion to the 1024-byte waveform record, the 64 extra samples are needed for proper clock switching between the Fast-In and Slow-Out portions of the FISO cycle.

The CCD has a Serial-Parallel-Serial (S-P-S) architecture. Each side has an 8 sample serial input "A" register, an 8 × 34 sample parallel storage "B" register, and an 8 sample serial output "C" register. Two such SPS sections are shown in Figure 3-5.

In addition to the SPS registers, a fourth register is provided between the input node and the A register. This register, called the Lead-in or L register, is what distinguishes each of the four sides of the CCD and causes them to sample 90° out of phase.

All the registers require two-phase, complementary-gate clocking to move the sample charge packets through the CCD. Hence, there are two A register clocks, two B register clocks, and two C register clocks. There are four L register clocks in order to produce the four sampling phases. There is also a Transfer In (TI) clock to shift samples from the serial A register into the B register and a Transfer Out (TO) clock to move them from the B register to the C register. All gates are driven with bipolar signals of nominally −5 V to +5 V.

Sampling into any of the CCD sides occurs on the falling edge of the first gate in the L register. The interfaces between the L registers and the corresponding A registers are identical. However, by varying the length and clocking of the L register, samples can be taken in different sides on each of the four L clock falling edges while still shifting all samples simultaneously into the A registers. The nomenclature of the sides corresponds to the number of the L clock which samples the charge packets into that side. Hence, a sample is taken first into side 1, then side 2, and so on.

When charge packets arrive at the end of the C register, they are converted to an output voltage by the

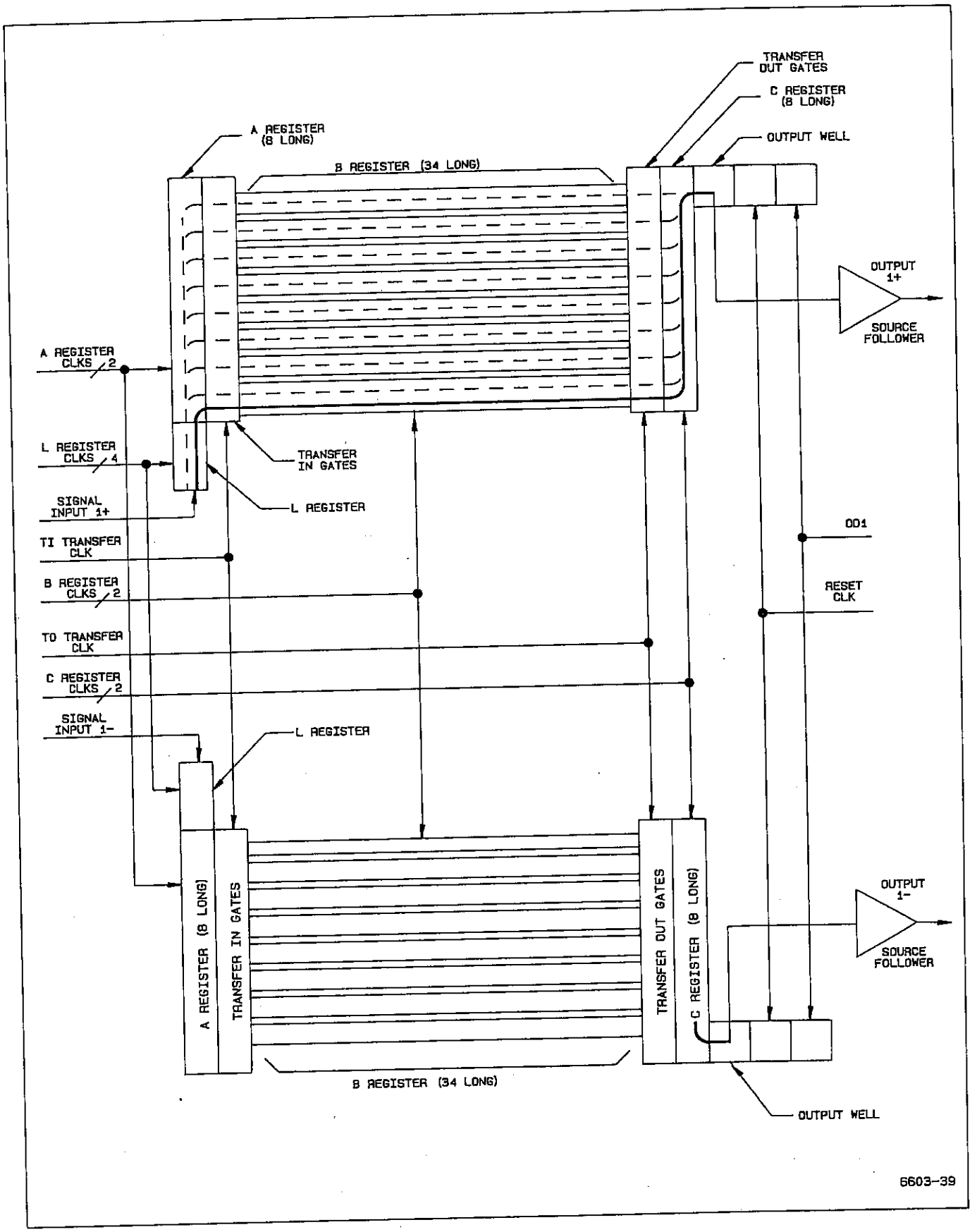


Figure 3-5. Simplified CCD architecture.

output source follower amplifiers. The $\overline{\text{RESET}}$ clock discharges the output wells between output sample intervals so that charge does not accumulate at the input to the source-followers.

In FISO mode, 8 samples are shifted down the serial input of A register at a clock period equal to 0.08 times the SEC/DIV setting. On every eighth clock cycle, the positive A2 clock pulse is replaced by a single positive TI pulse that moves all the charge packets into a transfer-in register at the head of the B register array. The A register is then empty and ready to accept new serial-in samples. The B register clocks run at 1/8 the speed of the A register clock rate so that the A register will be filled prior to each B register clock. In this way, the B register is filled with samples that are moved in parallel through the array. During this Fast-In portion of the input cycle, unneeded charges that arrive at the output C register due to the way the input signal is continually sampled (until a trigger occurs) are emptied from the CCD through the output diffusions (OD13 and OD24). When the Time Base Controller determines that the proper number of samples have been stored in the CCD after the trigger occurs, the mode changes to Slow-Out. The C register and RESET clocks then toggle at a constant 500 kHz rate to shift take samples out of the CCD to be digitized. The B register clocks pulse once during every eighth C register clock cycle to shift charge packets into the C register.

The Short Pipe mode of the CCD is in effect at SEC/DIV settings of 100 μs and slower. The CCD is operated at a continuous 500 kHz rate. Samples are shifted serially through the CCD via one B register channel only. The TI clock toggles continuously to move the sample charge packets from the first A register position into the active B register channel, shown in Figure 3-5 as the Short-Pipe Path.

All charge packets exit the CCD through the output diffusions (OD13 and OD24) which are biased at approximately 11 volts by operational amplifier U460A.

Clock Drivers

The Clock Driver integrated circuits internal to the CCD/Clock Driver hybrids develop the two "A" register clocks, the two "B" register clocks, the four "L" register clocks, and the transfer input (TI) and transfer output (TO) clocks for the CCD. The high-speed A, L, and TI drivers are differential class A drivers through thick-film load resistors on the hybrid. The B Register drivers are slower with active pull-up and pull-down totem-pole outputs similar to conventional TTL driver outputs. The TO gate is connected on the hybrid to the B2 gates and driven by the B2 driver output.

The L1 and L3 high-speed clocks are accessible at probe pins 18 and 19 of the hybrid devices. These pins (PL1 and PL3) are isolated from the actual CCD gates by internal 875-Ω series resistors. Terminate the signals into 50 Ω to view them. Using the standard 10 MΩ probe will cause the signals to have a displayed rise time of about 30 ns; the actual rise time internally is less than 2 ns.

Bias current for the Channel 1 high-speed drivers is set by the feedback circuit of U360B and Q375. The drivers are biased by injecting current into the IS input (pin 37). Increasing the current makes the LO level of the high-speed clocks more negative; decreasing the current raises the LO level. The HI level of the clocks is always within a few hundred mV of the +5 V supply to the hybrid. For controlling the negative clock level, the common-mode level of the L1 and L3 clocks at the PL1 and PL3 outputs is applied to the input of U360A. This level is compared to the midpoint between the +5 V and −5 V supplies. Operational amplifier U360A drives the base of Q375 to a level such that the current injected into IS sets the common-mode level of PL1 and PL3 equal to the voltage at pin 3 of U360A (the voltage supply midpoint value). Since the HI clock levels at PL1 and PL3 are approximately at the +5 V supply level, the LO levels of the clocks then are set to approximately the −5 V supply level. Bias stability is thereby maintained over temperature and component variations.

The logic inputs for the A, L, TI, and B drivers are all ECL levels from U470, the Phase Clock Gate Array. Resistor array R470 provides proper termination for the ECL logic inputs to the CH 1 Clock Drivers. Fine adjustment of clock timing for the L, A, and TI clocks is necessary to insure that the CCD transfers charge optimally, and that samples are taken at the right times in each of the four sides. The symmetry-delay integrated circuits provide this adjustability. These circuits sit between the ECL logic inputs to the hybrid and the clock driver integrated circuit. They accept the ECL level inputs and produce ECL level outputs which have several nanoseconds of adjustability of both the rising and falling edges. R442 through R449 are the calibration adjustments for the symmetry and delay of the L, A, and TI clocks. The dc level, "V1P," applied to U460B's input by U470, is the internal ECL threshold voltage of U470. This threshold is buffered by U460B and provided as the reference for the ECL inputs to the symmetry-delay integrated circuits. This provides stable logic switching times without the need for true differential ECL logic between U470 and U450.

"C" CLOCK DRIVERS. These are external clock drivers consisting of Q450, Q460, and associated components. They provide the necessary −5 V to +5 V clock swings for the CCD C register gates. Each driver is simply an inverting buffer which accepts TTL inputs from the Phase Clock Array. During the Fast-In portion of the FISO acquisition cycle, the outputs of both drivers are held HI by the Phase Clock Array. During the Slow-Out portion of the cycle, and at SEC/DIV settings of 100 μs and slower, the C Clock Drivers toggle at a 500 kHz rate with a 50% duty cycle. When toggling, the C2 output is 180° out-of-phase with the C1 output for normal two-phase clocking.

RESET DRIVER. This driver consisting of Q551 is identical to the C Clock Driver states. It takes the $\overline{\text{RESET}}$ signal input from U731C in the System Clocks circuitry (diagram 7). Like the C Clock Drivers, the Reset driver is driven HI during Fast-in and toggles at other times. The Reset driver output is held HI for only 200 ns of the 2 μs clock period.

−2 V Regulator

A −2 V supply needed to terminate all of the high-speed ECL signals on the Main circuit board is formed by U580B and Q580. The circuit is a simple series-pass regulator with R585 and R586 developing the −2 V reference for operational amplifier U580B from the −5 V supply. Feedback is through R587. Collector load resistors R486, R487, and R488 limit the power dissipation of Q580 and protect it from possible short circuits of the −2 V supply.

TRIGGERS AND PHASE CLOCKS

In this scope, the acquisition system continuously acquires input samples. When the user-specified number of "pretrigger" samples have been moved into the CCD arrays, the trigger system is allowed to recognize trigger events. Sampling of the signal input to the CCD arrays continues (with new samples pushing out old samples) until a trigger occurs. After the trigger, the number of "post-trigger" samples needed to fill the waveform record are moved into the CCD arrays and sampling is stopped. The acquired samples are then moved out of the CCD arrays, digitized, stored to memory, and displayed. The acquisition system then begins again to fill the "pretrigger window" for the next acquisition; and, when that has been done, the trigger system is enabled to look for the next trigger event.

The Trigger circuits (diagram 11) detect when the user-defined triggering conditions are met and then allow the acquisition to be completed. When the triggering signal limits defined by the user for slope, level, and variable holdoff are detected by A/B Trigger Generator U150, the resulting trigger output is applied to Trigger Logic Array U370, where triggering conditions of delay mode, delay time or delay events count, and optional trigger sources are taken into consideration. The Trigger Logic Array outputs several trigger-recognition and acquisition-control signals that cause the acquisition system to finish the "post-trigger" portion of the acquisition.

The Phase Locked Loop and CCD Phase Clock circuits (diagram 11) control sampling and shifting operations of the CCD/Clock Driver hybrid. The Phase Locked Loop synthesizes the 500 MHz sample clock driving the CCD Phase Clock Array. The CCD Phase Clock Array uses this "master" clock to generate other CCD clocks in accordance with mode data written to it from the System μP.

A/B Trigger Generator

The A/B Trigger Generator circuit, composed of U150 and associated components, provides for selection and analog-type trigger detection from five input signals for each of the A and B triggers. These are the CH 1 and CH 2 vertical inputs, the EXT 1 and EXT 2 trigger inputs, and the line-trigger input (A trigger only). Two multiplexers internal to U150 select one of these signals as the trigger source for A Trigger and one (excluding the LINE signal) for B Trigger. Source selection depends on the states of the $\overline{\text{SR0A}}$, $\overline{\text{SR1A}}$, and $\overline{\text{SR2A}}$ (source select—A trigger) lines for the A Trigger and on $\overline{\text{SR0B}}$, $\overline{\text{SR1B}}$, and $\overline{\text{SR2B}}$ for B Trigger. The appropriate select bits are written into register U140 by the System μP whenever the operator makes a triggering condition change using the trigger source menus.

Control data from the System μP defining trigger mode, trigger coupling, and trigger slope are clocked serially (one bit at a time) from the CD (control data) line into two storage registers internal to U150. Clocking the $\overline{\text{CCA}}$ (control clock A) line moves the setup data to the A control register, while clocking $\overline{\text{CCB}}$ moves data to the B control register. When the control data has been loaded, each trigger circuit begins comparing its selected input signal to the user-defined trigger level for that trigger channel.

When the defined triggering criteria are met for either A or B, the associated trigger outputs (ATG, $\overline{\text{ATG}}$ for A Trigger; BTG, $\overline{\text{BTG}}$ for B Trigger) will go to their asserted (true) states. The exception is when the A Trigger holdoff has not finished (ATHO is still HI). When the holdoff ends, however, the next trigger event on the selected A Trigger input will assert the A Trigger output gates.

Each differential trigger gate is inverted and current buffered by a pair of differential transistors that allow quick response to the trigger edges by Trigger Logic Array U370.

Trigger Logic

The Trigger Logic circuit consists primarily of Trigger Logic Array U370. The Trigger Logic Array provides final trigger-source selection; trigger-point delays, delayed either by a specified amount of time or by a specified number of events; and ramp-control signals to the Jitter-Correction circuitry for resolving trigger-point ambiguities. The Trigger Logic Array also produces the trigger and external clock signals necessary to control operations of the CCD Phase Clock circuit.

The three enable inputs to U370, E1B (A3), E2B (WR), and E3B (ACQSEL), are all set LO whenever writing to addresses between 6080h and 6087h to enable the address inputs (A0, A1, and A2). The choice of eight addresses between 6080h and 6087h provides for different operating requirements of the Trigger Logic Array.

Depending on the address written to, one of the following actions may occur:

Mode control data may be loaded into the internal mode register.

The internal events and delay counter low-byte or high-byte of the number of events to be counted or delay may be loaded.

Various strobes used for internal control of the Trigger Logic Array may be generated.

Table 3-5 shows the action taken for each address selected.

Table 3-5
Trigger Logic Array Addresses
(6080h-6087h)

Address Bits			Circuit Operation Initiated
A2	A1	A0	
0	0	0	Restart Acquisition
0	0	1	Force Manual Trigger
0	1	0	Load Mode Control Data from M0-M7
0	1	1	Latch Delay Counter Low-Byte from M0-M7
1	0	0	Latch Delay Counter High-Byte from M0-M7
1	0	1	Load Delay Counter from Delay Latches
1	1	0	Select Events in FISO, Delay by Events, or Short Pipe
1	1	1	Reset All Latches

As previously mentioned, U370 provides final trigger-mode and source selection, dependent on data written from the System μP to a control register within U370 at address 6082h. The mode control data byte loaded from the M0-M7 input bus is built by the System μP and applied to the M0-M7 (mode) inputs from serial-input register U270 (diagram 5) via the GAD0-GAD7 bus lines. The data byte defines the A Trigger source, B Trigger source, Record Trigger source, Jitter Trigger source, and whether a single event or multiple events are needed to produce a trigger. Bit definition is shown in Figure 3-6.

After the control data byte is loaded and the acquisition is restarted, Trigger Logic Array U370 waits for EPTHO (end of pretrigger holdoff) to go HI at pin 28, indicating that the acquisition system has sampled the "pretrigger" points and is ready to complete the acquisition. With EPTHO set HI, the trigger logic begins watching the trigger source (as defined by the control data byte), waiting for a trigger event to occur.

Operation of the Trigger Logic Array is very sequential in the way it functions in the various trigger modes. An example is illustrated in the sequence of events for B RUNS AFTER trigger mode.

1. The System μP loads the "delay count" and "control mode" registers, then starts the acquisition (indicated by setting RSTACQ HI at TP370).

2. The Trigger Logic Array watches for EPTHO at pin 28 to go HI; signaling that the defined number of pre-trigger points have been sampled.

3. With EPTHO HI, the Trigger Logic Array watches MTG and $\overline{\text{MTG}}$ (main trigger gate) for an A trigger event to start the delay counter. When a trigger occurs, JTRIG (jitter trigger) is generated, starting the jitter-correction circuits (via the RAMP and $\overline{\text{RAMP}}$ signals).

4. The defined delay count is decremented to zero by the DELCLK (delay clock) signal on pin 67 from Phase Clock Array U470. If the mode were A Delayed by B Events, the B Trigger events would be used to decrement the delay counter.

5. In this example, when the internal Delay count reaches 0, a RTRIG (record trigger) is generated for B RUNS AFTER. RTRIG is the "record trigger" point on the displayed waveform. If the mode were B TRIG AFTER, the Trigger Logic Array would begin watching for a B Trigger to occur on the DTG and $\overline{\text{DTG}}$ input pins (Delay Trigger Gate).

6. Time Base Controller U670 (diagram 8) counts the post-trigger samples as they are acquired. When the required count is reached to complete the acquisition, it resets EPTHO to LO and further triggers from the Trigger Logic Array are prevented from being generated.

The Time Base Controller then starts moving digitized samples to the Acquisition Memory and, when finished, tells the System μP that the acquisition is done. The System μP may then restart the whole process again for the next acquisition by writing appropriate data to the various trigger registers.

In external clock mode, the differential EXTCK and $\overline{\text{EXTCK}}$ (external clock) signals to the Phase Clock circuit replace the normal master-clock (MCLK) signal and allows the B trigger events to be used as the events delay source.

CONTROL DATA BYTE

A2	A1	A0	M7	M6	M5	M4	M3	M2	M1	M0
0	1	0	JT1	JT0	RT1	RT0	ONEVNT	BT0	AT1	AT0
1	1	0	DON'T CARE					EVDEL	SELEVENTS	ABTRIG

JITTER TRIGGER BITS

JT1	JT0	SOURCE
0	0	A TRIGGER
0	1	B TRIGGER
1	0	END EVENTS
1	1	B TRIGGER

RECORD TRIGGER BITS

RT1	RT0	SOURCE
0	0	A TRIGGER
0	1	END DELAY TIME
1	0	END DELAY EVENTS
1	1	B TRIGGER

ONE EVENT BIT

ONEVNT	EVENTS=1
0	NO
1	YES

B TRIGGER BIT

BT0	SOURCE
0	DELAYED INST. TRIGGER
1	WORD TRIGGER OPTION

A TRIGGER BITS

AT1	AT0	SOURCE
0	0	MAIN INST. TRIGGER
0	1	VIDEO TRIGGER OPTION
1	0	WORD TRIGGER OPTION
1	1	A*B TRIGGER

DELAY BY EVENTS & TIME BIT

EVDEL	MODE
0	NOT DELAY BY EVENTS AND TIME
1	DELAY BY EVENTS AND DELAY BY TIME

SELECT EVENTS BIT

SELEVENTS	MODE
0	FISO ONLY, NO EVENTS
1	DELAY BY EVENTS OR SHORT PIPE

AB COMBINATIONAL TRIGGER

ABTRIG	SOURCE
0	A AND B
1	INTERNAL MODE ONLY

6603-40A

Figure 3-6. Trigger Logic Array Control Data Byte.

The $\overline{\text{A TRIG}}$ and $\overline{\text{R TRIG}}$ outputs from Q287 and Q288 are TTL-buffered versions of the corresponding trigger signals and are routed to rear-panel BNC connectors.

Phase Locked Loop

The Phase Locked Loop circuit synthesizes the 500 MHz clock used by the Acquisition System. It consists of Phase/Frequency comparator U381 amplifier U580A, a voltage-tuned tank circuit, and a divide-by-50 counter internal to Phase Clock Array U470. The tank-circuit resonant frequency is set by the value of voltage-controlled capacitors CR580 and CR582. The resulting clock is divided by 50 by the counter and is applied to the phase-frequency detector U381 on the TENREF line. The TENREF signal is compared to the reference clock 10 MHz, and any phase or frequency error appears at the output of U381 as variable width pulses. These pulses are integrated by U580A to produce a dc voltage that represents the phase difference (fast or slow) and magnitude of error between the 10 MHz clock and the divided down master clock. This is the frequency-control voltage and varies the capacitance of varactor diodes CR580 and CR582, part of the tank circuit formed by the circuit board delay line, CR580 and CR582. The tank is tuned by the control voltage so that the master clock frequency is precisely 50 times the reference frequency.

CCD Phase Clock

The CCD Phase Clock generates properly phased and frequency-related clocks that control most of the Acquisition system. These functions include moving samples into the CCD arrays, shifting within the arrays, jitter-correction control, peak-detection control, and trigger-delay clock generation. These clocks are derived from the 500 MHz master clock generated by the internal oscillator and the Phase Locked Loop circuit.

Two operating modes exist for the CCD arrays; FISO (fast-in, slow-out) and Short-Pipe. The Phase Clock circuit is set up to generate proper clocking signals for either mode by loading data into Gate Array Control Register U270 (diagram 5). This data is applied to U470 on the CC0-CC4 (chip control 0-4) lines and on the PDOFF (peak detector off) line. The PDOFF line enables/disables the peak-detector output lines (PD1, $\overline{\text{PD1}}$, PD2, and $\overline{\text{PD2}}$) and thus peak detection mode (see that description). The CC4 input controls whether the scope uses a non-Delay- or a delayed-by-time trigger source. If Horizontal mode is B and B Trigger Mode is B delay-by-time, is in normal (or delay by time trigger mode. When set high, the phase clock will choose the RTRIG signal as the trigger source for delay by time. If set low, the phase clock will choose JTRIG as the source. The CC0-CC3 inputs control operating mode and clock selection as shown in Table 3-6.

FISO MODE. As explained in the CCD description, each CCD is made up of two identical differential channels using a serial-parallel-serial (SPS) structure. Samples are moved into and shifted within the CCD arrays using properly phased, overlapping clocks. Figure 3-5 shows a basic CCD structure (see CCD description, diagram 10).

Depending on which of the four sides of the CCD is being acquired, the corresponding sample gate (L1, L2, L3 or L4) will go HI. This moves the present level of the input signal into the input well of the CCD arrays. Before the sample gate returns LO, the ϕ1A (phase A1 register) clock goes HI and the charge is shared by the adjacent cells (input and ϕ1). When the sample gate returns LO, all charge moves to the ϕ1 cell. The ϕ2A clock then goes HI and charge is distributed into both the ϕ1 and ϕ2 cells. When ϕ1 returns LO, all charge will move into the ϕ2 cell.

When 8 samples have been acquired in the A register, the TI (transfer into B) clock moves all 8 samples from the ϕ1A cells in parallel into the B register. The two phases of the B clocks shift samples down the 8 parallel B registers in a manner similar to that just described for the A register but at 1/8th the rate. The $\overline{\text{TTLB1}}$ clock (TTL-version of B clock ϕ1) is output to the Time Base Controller and allows it to keep track of how many samples have been acquired (in multiples of 32). This allows the Time Base Controller to know when the proper number of "pretrigger" points have been acquired and when to enable the Trigger Logic Array.

Once enabled, the Trigger Logic Array begins counting its predefined delay while samples continue to be acquired. The DELCLK (delay clock) output to the Trigger Logic runs at one-half the sample-clock rate, allowing the Trigger Logic to complete any defined delay. When delay is done, the JTRIG and RTRIG signals may be generated. When the JTRIG occurs, the RAMP and $\overline{\text{RAMP}}$ signals from the Trigger Logic start the Jitter-Correction Ramps. The JTRIG signal to U470 causes the TL0 and TL1 (trigger location-bits 0 and 1) bits to latch the phase (HI or LO) of the L1 and L2 clocks, defining in which quarter of the cycle the trigger event occurred. The internal slow-ramp logic circuitry of U470 becomes enabled and, on the next two edges of the master clock, asserts the two pairs of slow-ramp (SLRAMP) outputs. These outputs reverse the charge direction of the Jitter-Correction Ramp circuits (diagram 12) and start the Jitter-Correction Counters (diagram 13) on opposite edges of the master clock. See those descriptions for further information on trigger-jitter correction.

Depending on trigger mode, the RTRIG (record trigger) line will be asserted some time after JTRIG occurs. RTRIG is synchronized to the B-register clock and is output to the Time Base Controller on the SYNTRIG (synchronous trigger) line, telling it to start counting post-trigger samples. The RTRIG also loads a register internal to U470

Table 3-6
Phase Clock Array Control Lines (CC3 through CC0)

SEC/DIV Setting	Control Bits				Mode
	CC3	CC2	CC1	CC0	
EXT CLK	1	1	0	0	
100 ns and faster	0	1	0	1	FISO
200 ns	0	1	1	0	FISO
500 ns	1	0	0	1	FISO
1 μs	1	0	1	0	FISO
2 μs	1	0	1	1	FISO
5 μs	1	1	0	1	FISO
10 μs	1	1	1	0	FISO
20 μs	1	1	1	1	FISO
50 μs	0	0	0	1	FISO (Short-Pipe Clock Source)
100 μs and slower	0	1	1	1	Short-Pipe

with the present sample count to locate the trigger event (explained later). When the Time Base Controller has completed the post-trigger count, it will set SO (slow out) HI, switching the Phase Clock Array mode from "Fast In" to "Slow Out" mode. The various phase clocks are now derived from the 1 MHz 2XPC clock (from the Time Base Controller) instead of the 500 MHz master clock, and samples are shifted out of the CCD arrays at the A/D conversion rate.

Outputs TL0-TL4 (trigger location bits 0 through 4) define the trigger location within ±1/2 of a sample interval and allow the extra samples taken at the beginning and end of the CCD sample array contents to be discarded. Defining and discarding these samples is done because the trigger event may occur at any of 32 locations within the four A registers. Outputs TL2-TL4 locate the trigger at one of the eight sample positions within the A register, allowing samples before the start of the waveform to be discarded. Outputs TL0 and TL1 define trigger position within the sample interval to one of the four sides (L1, L2, L3 or L4) by sampling the phase of the L clocks when the trigger occurred.

SHORT-PIPE MODE. A second acquisition mode, Short-Pipe mode, is used at SEC/DIV settings 100 μs/div and slower. In Short-Pipe mode, the φA2 clock that transfers samples down the input (A) register is disabled; and instead, the TI (transfer into B array) clock shifts samples straight down the first register of the B array to the output well. Sampling occurs at 2 MHz in Short-Pipe mode (500 kHz each side of the CCD array) as the various phase clocks are derived from the 2XPC clock. Trigger delays are generated at the SDC (slow-delay clock) rate since Short-Pipe mode connects the DELCLK output to the SDC input. Since sampling is occurring at a 2 MHz rate and the SEC/DIV is set so that a sample rate slower than this is required, some of the samples must be discarded. The discrepancy is resolved by Time Base Controller by counting and discarding the proper number of samples between those it allows to be saved. This allows effective sample rates much lower than the actual 2 MHz rate and, by routing the SDC signal to DELCLK, allows the trigger delays to be counted in terms of effective sample events.

In FISO mode, the $\overline{\text{TTLB1}}$ (TTL-level phase B1) signal runs at 1/8 of the A-register clock rate and is used by the Time Base Controller to keep track of how many FISO samples have been taken. Each $\overline{\text{TTLB1}}$ clock indicates that 8 sample intervals have occurred. In Short-Pipe mode, the $\overline{\text{TTLB1}}$ clock runs at the A-register clock rate. By using the $\overline{\text{TTLB1}}$ count and the TL0-TL4 data, the Time Base Controller (U670, diagram 8) can precisely determine when the acquisition is finished.

TTLC2 is a TTL version of the phase 2 clock for the C (output) register and runs at all times except during RESET. This is one of the signals required by the System Clock Generators for producing correctly timed Output Sample Clocks to the CCD Output circuitry (diagram 14) and the $\overline{\text{RESET}}$ clock to the CCD arrays.

JITTER CORRECTION RAMPS

The Jitter Correction Ramps located on diagram 12 are a portion of two dual-ramp timing circuits used to detect and measure the time difference between a trigger event and the sample clock. This information is needed when doing acquisitions at SEC/DIV settings greater that 100 ns to correctly place the data points obtained on different trigger events. The Jitter Correction Counters are located on diagram 13.

Jitter Correction Ramps

Operation of the RAMP1 and RAMP2 circuits is identical; therefore, only the RAMP1 Jitter Correction circuit will be described. Both Jitter Correction Ramps are initiated by the same trigger event, but they are switched to their slow-discharge mode on opposite edges of the sample clock. By switching on opposite edges, the trigger point has two distinct references which define the trigger point, allowing the System μP to detect and correct for metastable states of the trigger recognition logic.

The ramp generator consists of a constant current source used to rapidly charge an integration capacitor when the trigger event occurs and a second current source used to discharge the capacitor (more slowly) after the proper edge of the sample clock occurs. The fast-charge time is the actual time from the trigger event to the appropriate sample-clock edge. The time it takes the slow-discharge mode to discharge C491 gives a numerical representation (counted) of how high the ramp level reached when C491 was fast charging; and therefore, the time of the fast ramp.

Fast charging rate is determined by the constant current source formed by U590A, Q493, and associated components. The charging current is nominally 50 mA through R590, R591, R593 and Q493. The voltage drop across the resistors balances the +7.5 volt reference at pin 2 of U590A and keeps Q493 turned on just enough to maintain the balance at the operational amplifier inputs.

This charge current is switched through either Q491 or Q492, depending on whether the ramp should be ramping down slowly or ramping up quickly. When waiting for a trigger to occur, the SLRMP1 (slow-ramp 1) will be LO, turning Q491 on. Charging current from Q491, which would normally charge integration capacitor C491 (and the 50 pF circuit-board capacitor), is shunted to −5 volts by Q490, which is turned on by a HI $\overline{\text{RAMP}}$ fast ramp) signal applied to its base.

RAMP CLAMPING. The clamping circuit made up of U590B, CR490, and associated components, holds the ramp summing-node voltage (collector of Q490) at zero volts while the circuit is waiting for a trigger to occur (signaled when RAMP and $\overline{\text{RAMP}}$ go to their true states). The summing-node voltage is applied to U590B on pin 6 where it is compared to the zero-volt clamp level (ground) on pin 5. When the summing node attempts to go below ground while Q490 is on, U590B will conduct more to maintain the balance at the input pins, thereby clamping the summing node at zero volts via R592 and CR490.

Transistor Q380 and its associated components clamp the positive peaks of both ramps at +3.2 volts via CR491. This clamping takes place at SEC/DIV settings slower than 100 ns/div because the SLRMP signal doesn't occur soon enough after the RAMP signal starts the ramp to reverse the ramp slope before the +3.2 V level is reached.

RAMP SWITCHING. When Trigger Logic Array U370 (diagram 11) detects that a trigger event has occurred, it sets the RAMP and $\overline{\text{RAMP}}$ signals to their active (true) states. The LO $\overline{\text{RAMP}}$ signal turns Q490 off to allow the integration capacitor to begin a fast charge, and the HI RAMP signal turns Q392 on to reverse bias CR490 and remove the clamp circuit from the summing node.

The charging current now linearly charges C491 and the circuit board capacitance positive (holding STOP1 LO through U490) until the proper edge of next sample clock occurs (see Figure 3-7). This switches the SLRAMP1 and $\overline{\text{SLRAMP1}}$ signals to their true states, turning off Q491 and turning Q492 on.

With Q492 on, the charging current is routed through R497, producing a HI START1 signal and enabling the RAMP1 Jitter Correction Counter circuit (diagram 13). Since Q491 is now off, C491 begins the slow-ramp discharge through Q495 and R493. When the voltage held on C491 crosses the switching threshold of U490, STOP1 is switched HI to turn off RAMP1 Jitter Correction Counter at the proper count.

At the time of calibration, the JIT1 GAIN (jitter gain—ramp 1) value is set to the base of the discharge current source transistor, Q495, so that the ratio between charging rate and discharging rate is 1250:1 (approximately 20 mA from the charging current source to approximately 16 μA discharge current from Q495). The slow discharge time of C491 allows the RAMP1 Jitter Correction Counter to convert the peak amplitude of RAMP1 (dependent on the time that C491 was allowed to fast charge) into a count relating trigger-event position to the sample-clock edge.

After the Jitter Counter has been read, the RAMP, $\overline{\text{RAMP}}$, SLRAMP1, and $\overline{\text{SLRAMP1}}$ signals will be reset to their inactive states. This again clamps the summing-node voltage at zero volts and reapplies the charging current to the node in preparation for the next trigger event.

RAMP2. As mentioned earlier, the RAMP2 Jitter Correction circuit is running simultaneously, referenced to

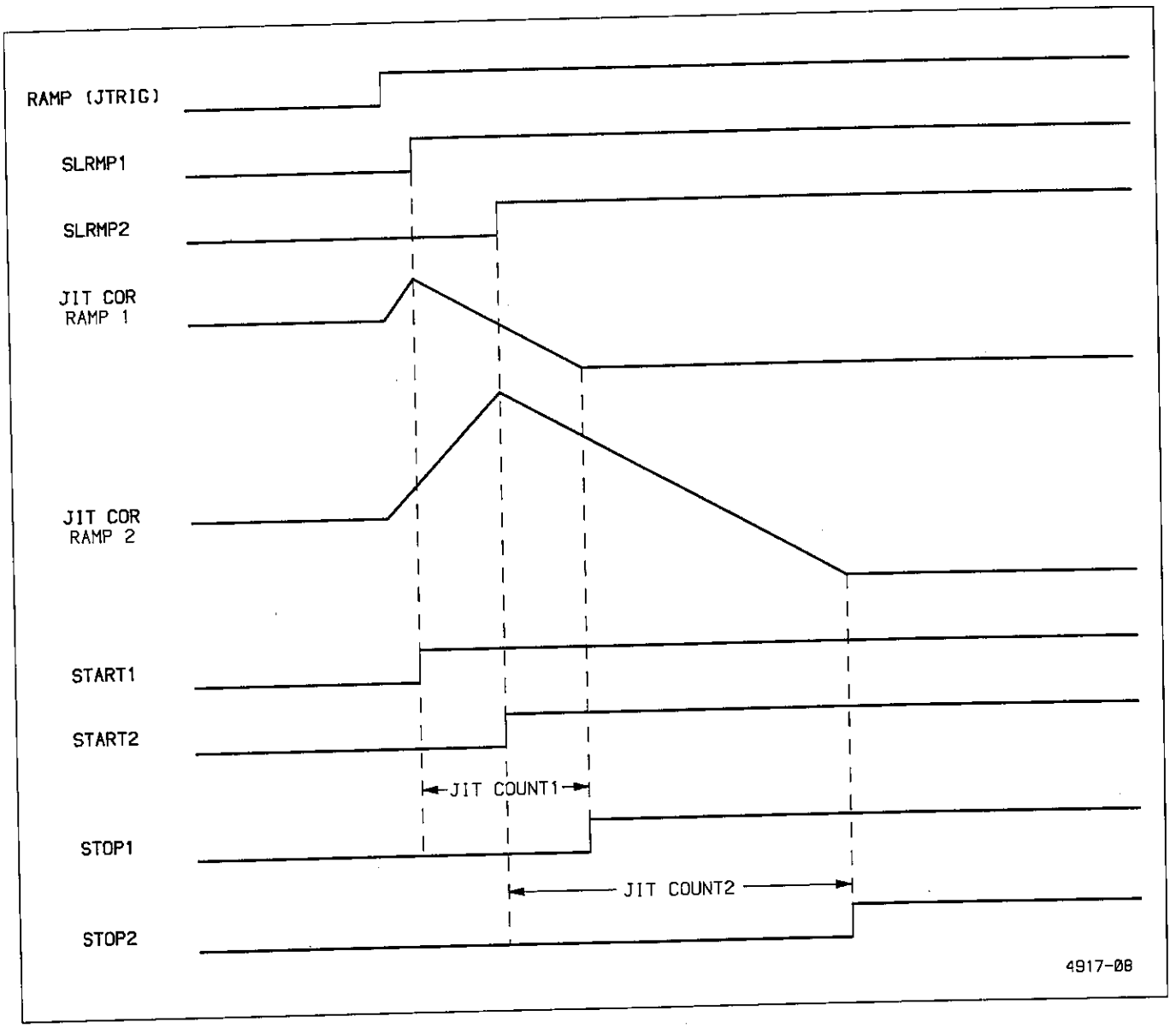


Figure 3-7. Jitter Correction waveforms.

the opposite edge of the sample clock. The RAMP2 Jitter Correction Counter produces a count defining the trigger point relative to the opposite edge of the sample clock. Since both ramps have a possibility of an error in their slow-ramp starting times (due to metastable switching of the SLRAMP1 and SLRAMP2 signals) there will always be a chance of error present in the trigger-position count. The count from both ramps is checked, and the value closest to the nominal midrange count will be used by the System μP when placing the repetitively sampled data points. If both counts are in error, that acquisition is discarded.

TRIGGER HOLDOFF, JITTER COUNTERS, AND CALIBRATOR

Circuitry shown in diagram 13 performs a variety of functions.

The Trigger Holdoff circuits allow a delay to occur between the occurrence of a triggering event and when the A/B Trigger Generator is allowed to recognize another trigger event. Variable Holdoff can help the user prevent double triggering on aperiodic signals (such as complex digital words).

The RAMP1 and RAMP2 Jitter Correction Counters measure the time difference between the asynchronous trigger event and the actual sampling point of the waveform data. That information is needed by the System μP to place the random samples taken in REPET acquisition mode correctly with respect to data points taken in the previous acquisitions to fill the waveform record.

The Calibrator circuit generates a square-wave output having precise amplitude and frequency characteristics. The CALIBRATOR signal provided at the front-panel connector is useful for adjusting probe compensation and verifying VOLTS/DIV and SEC/DIV calibration.

The Side Board Address Decoder included in the circuitry is used by the System μP to enable the appropriate register or buffer on the Side board to read the Jitter Correction Counters, select the Holdoff Time, and communicate with the Front Panel μP.

Trigger Holdoff

The Trigger Holdoff circuit consists of a trigger-enabled, constant current source (actually one of three selectable sources added to a small permanent source) used to linearly charge a capacitor (one-of-two selectable cap values). The resulting integrator output is a linear ramp whose slope depends on the current-source and integration-capacitor selection. The ramp is applied to the Holdoff Comparator where it is compared to the user-definable (front-panel pot) holdoff-reference level. When the charging ramp crosses that level, the ramp rapidly discharges (resets) and ends the holdoff condition.

Holdoff Select

The Holdoff Select circuit, under System μP control, determines which of the Holdoff Current Sources and which of the integration capacitors will be used to produce the holdoff ramp. Its outputs are set by the microprocessor by writing data into Holdoff Register U762, residing at address 620Ch. Output bits HO0 through HO2 (holdoff control bits 0-2) enable their corresponding current-source transistor when HI. Bit HO3 is used for selection of the integration capacitor. The $\overline{\text{FPRESET}}$ bit allows the system processor to reset the Front Panel μP (diagram 3).

Buffer U761, residing at read location 602Ch, allows the System μP to check the holdoff circuit setup and to monitor the status of the A Trigger (ATG) and trigger holdoff (ATHO) bits.

Holdoff Current Sources

The Holdoff Current Sources provide the constant currents used to charge the integration capacitors (producing a linear ramp). The circuit consists of four transistor current sources, three of which may be turned on or off under control of the Holdoff Select circuit.

The bases of the four current-source transistors, Q761, Q771, Q772, and Q773, are held one diode-drop below +5 V by CR772 and R773. This results in precisely +5 V being present on the emitter of any conducting current-source transistor. The amount of current is set by the value of emitter resistor(s). Transistor Q773 will always be on while the other three current-source transistors can be turned on or off by the HO control bit via the associated emitter diodes. A LO at the cathode of one of these diodes will disable the associated current source by reverse biasing the transistor junction; a HI at the cathode of a diode enables the charging-current source via the associated emitter resistor.

Charging Capacitor Selection

The Charging Capacitor Selection circuit composed of Q783, Q782, and associated components, selects the integrating capacitance. The magnitude of the charging current from the selected current source, in combination

with the capacitance value, of the integration capacitor, determines charge rate (slope) of the holdoff ramp; and thereby, the holdoff time. Table 3-7 illustrates the holdoff time as a function of the selected current source and charging capacitor.

Charging current is stored on capacitor C882 when holdoff intervals less than or equal to 10 μs are desired. For longer holdoff periods, capacitor C881 and C885 are placed in parallel with C882 by turning Q782 on. Transistor Q782 turns on when HO3 (holdoff select 3) is LO, turning Q783 off. This pulls the gate of Q782 high and turns it on, placing the parallel combination of C881 and C885 in parallel with C882. Due to the relative capacitance ratios (1000:1), C881 is the dominant integrating element in the three-capacitor parallel combination.

Holdoff-Ramp Comparators

Two Holdoff-Ramp Comparators, U871 and U881, watch the holdoff ramp. Comparator U871 compares the ramp level to the user-defined reference level while U871 compares it to a predefined "end-of-holdoff" level.

Initially, a HI on the $\overline{Q}$ output of Holdoff Logic flip-flop U872A keeps Q781 turned on. The integration capacitors are discharged, and all the charging current is being shunted away from the capacitors through Q781. The user-definable holdoff reference applied to U871 pin 2 via R863 will always be more positive than this discharged level, so the output of U871 applied to the Holdoff Logic will be HI. This removes the reset from the Holdoff Logic flip-flop U872A and enables the occurrence of a trigger event (ATG going HI) to clock it.

When a trigger event occurs, discharge transistor Q781 turns off, allowing the selected integrating capacitors to charge. When the charging ramp reaches the user-defined HOREF (holdoff reference) level, the output of ramp comparator U871 will go LO. This resets flip-flop U872A of the Holdoff Logic which, in turn, turns Q781 back on.

The low-impedance path through Q781 discharges the integration capacitor very rapidly. When this discharging ramp crosses the −4.6 volt level (defined by R887 and R888), the output of U881 will go LO, resetting the Holdoff Logic circuit. This ends the holdoff pulse and allows the next trigger to be accepted.

Transistor Q781 remains on until the next trigger event, at which time the cycle repeats itself. Propagation delays through the Analog Trigger and the Record Trigger devices ensure that the discharging ramp will always reach the −5 V level before another trigger event can start the next holdoff ramp.

Holdoff Logic

The Holdoff Logic initiates and controls the holdoff ramp and produces the holdoff pulse controlling the delay between one trigger event and the next. It starts the holdoff ramp when a trigger event is detected, begins ramp discharge when the user-defined HOREF level is reached, and ends the holdoff pulse when the ramp crosses the "end-of-holdoff" level.

Initially, the Set and Reset inputs of U872A will be HI, allowing the flip-flop to watch the ATG (analog trigger) line for a trigger event. While it is waiting, its $\overline{Q}$ output will be HI, keeping Q781 on and the integration capacitors discharged.

When an ATG occurs, the HI level at the input of the flip-flop is clocked to the Q output while the $\overline{Q}$ output goes

Table 3-7
Holdoff Delays vs Current Source/Charging Capacitor Combinations

Charging Capacitor	Holdoff Delay Range				
	Current Source				
	909 μA	90.0 μA	9.09 μA	827 μA	
1000 pF	10 ns - 100 ns	100 ns - 1 μs	1 μs - 10 μs		DELAY
1.1 μF	10 μs - 100 μs	100 μs - 1 ms	1 ms - 10 ms	10 ms - 100 ms	

LO. This LO turns Q781 off and allows the selected current source(s) to charge the capacitors. At the same time, the LO is applied to pin 10 of U872B, forcing its Q output HI. This is the ATHO (analog trigger holdoff) signal and indicates that an analog trigger has occurred. This signal is applied to A/B Trigger Generator U150 (diagram 11) to prevent it from recognizing another trigger until the holdoff time ends.

As the charging ramp reaches the user-defined (front-panel Holdoff pot) reference level, the output from comparator U871 will go LO. This $\overline{\text{CROSS}}$ (reference crossing) level is applied to U872A and resets the flip-flop. The $\overline{Q}$ output, now HI, turns Q781 on and begins discharging the ramp at a rapid rate. The HI $\overline{Q}$ output from U872A removes the Set level from U872B and allows the ENDHO (end of holdoff) level from U881 to reset the ATHO level LO when the discharging ramp reaches −4.6 volts.

As mentioned earlier, propagation delays in the A/B Trigger Generator and the Trigger Logic Array ensure that another trigger (ATG) will not occur until Q781 has discharged the integration capacitors fully to −5 V. This ensures that holdoff ramps always start from a known point, and thus maintains holdoff stability.

The width of the ATHO pulse represents the time from which one analog trigger event was accepted to when the next trigger event is allowed (next acquisition record). By varying this time (front-panel Holdoff control) the displayed waveform may be adjusted to exclude undesired trigger events (which may cause display instability).

Jitter Correction Counters

The RAMP1 and RAMP2 Jitter Correction Counters convert the discharge time of their associated Jitter Correction Ramps to binary numbers relating trigger-event positions to the edges of the sample clock. Since operation of both Jitter Correction Counters is identical, only the RAMP1 Jitter Correction Counter will be described.

The RAMP1 Jitter Correction Counter is a twelve-bit counter that is started and stopped by signals from the RAMP1 Jitter Correction circuit. It counts the 40 MHz clock pulses over the interval when the Jitter Correction Ramp is discharging, thus converting the peak value of the ramp to a binary number. Since that value is directly proportional to the time difference between a trigger event and the next sample-clock edge, the number derived by the counter gives a precise time measurement of where the trigger occurred with respect to the sampled data. That information is used by the System μP to correctly place the random-sampled data points obtained in REPET acquisition mode with respect to the previously acquired random data points as the waveform record is filled.

Initially, the upper eight bits of the RAMP1 Counter (composed of U852A and U852B) are held reset by the HI from pin 6 of U841A, and the lower four bits are reset by the LO from pin 5. When the START1 (start counter 1) input goes HI (signaling start of the slow discharge of integration capacitor C491, located on diagram 12), the rising edge of the next 40 MHz clock pulse will enable the counter by clocking the Q output of U841A HI. The Q output of the "stop" flip-flop U841B is LO and enables U851B to pass rising-edge clock pulses to U844 at a 40-MHz rate.

The counter increments until the RAMP1 Jitter Correction circuit detects that the discharge threshold has been crossed. When this occurs, STOP1 (stop counter 1) applied to U841B will go HI. The next rising edge of the 40 MHz clock disables U851B via U841B and stops the counter.

The System μP may then read the counter contents via U752 at address-decoded location 620Eh and via U750 at 620Ah. Counter contents for the B Jitter Correction Counter may be read at location 620Fh and 620Ah.

When the jitter ramps are reinitiated (in preparation for the next trigger event), the START1 and STOP1 signals will return LO. The next rising edge of the 40 MHz clock will reset the Jitter Correction Counter by clocking pin 6 of U841A HI.

Address Decoder

Address Decoder U781 monitors the address bus to determine when various buffers and registers on the Side board are to be enabled for communication with the System μP. Table 3-8 illustrates this decoding.

Table 3-8
Side Board Address Decoding

Address (hex)	Selects or Enables
6208	LED Register
6209	Front-Panel Register
620A	Read lowest four bits of both Jitter counters
620B	No connection
620C	Write/Read Holdoff Register
620D	Set Holdoff Flip-Flop
620E	Read Jitter Correction Counter 1
620F	Read Jitter Correction Counter 2

Calibrator

The Calibrator circuit is composed of U731, U831, Q831, and associated components. Output frequency is set by the CALCLK signal from the Time Base Controller (diagram 8). The output frequency follows the SEC/DIV setting from 50 ns/div to 20 ms/div and is set to display from 2.5 to 10 calibrator cycles across the ten graticule divisions over those settings. This feature allows quick and easy verification of the acquisition time base rates. The Calibrator circuitry is essentially a voltage regulator that is switched off and on, producing a square-wave output signal at the CALIBRATOR loop.

When the CALCLK (calibrator clock) signal, at the base of U831D (applied via R885) is LO, U831C (configured as a diode) is forward biased. This shunts bias current away from Q831, keeping it turned off. When Q831 is off, the front-panel CALIBRATOR output is pulled to ground potential, through R831, thereby setting the lower limit of the CALIBRATOR square-wave signal.

As the CALCLK signal goes from LO to HI, the base of U831D is pulled HI, reverse biasing U831C. Bias current for Q831 now flows through R834 and R835, turning it on. The voltage at the emitter of Q831 rises to a level of +2.4 volts, determined by the voltage regulator composed of U731, U831A, U831B, Q831, and associated components. This regulated level is divided down to +400 mV p-p, by the resistive divider formed by R832 on the side board and R102 on the main board, and applied to the front-panel CALIBRATOR loop at an effective output impedance of 50 Ω.

CCD OUTPUT

The CCD Output circuits (diagram 14) convert the four differential output signals from each CCD into single-ended signals for subsequent A/D conversion. The single-ended analog voltages are applied to Track-and-Hold circuits where they are held until the time-multiplexed A/D Converter digitizes the stored samples.

Gain-Cell Amplifiers

There are eight identical Gain-Cell amplifiers (two on each of four Gain-Cell circuit boards) used to convert the eight differential CCD array outputs (four for each channel) to single-ended signals for A/D conversion. Operation of the Channel 1, Side 1 Gain-Cell amplifier is described.

CCDO11 signal outputs from U450 pass to the Gain-Cell board (diagram 14A), where they are applied to the bases of U111A, U111B, U111C and U111D via R113 and R114. Transistors U111A-U111D, along with current-source transistors Q111 and Q112, form a variable-gain differential- current amplifier. The differential current at the collectors of U111B and U111C is equal to the differential current through U111A and U111D, multiplied by the ratio of the dc current for the Q112 current source to that of the Q111 current source. Since the Q111 current is set by the fixed bias on the its base-emitter circuit, the gain adjustment of the amplifier is controlled by the dc voltage at the base of Q112, which is controlled by the System μP via the DAC system. The gain set is dependent on a calibration constant determined at instrument self-calibration.

The collectors of U111C and U111D are connected to operational amplifier U118A, which is configured as a differential-input, single-ended output transresistance amplifier. The connection of R115 to the +8.5 V supply causes the output of U118A to be level shifted to +8.5 V. The resulting output at pin 1 of U770A (GC11) is a level-shifted, amplified, single- ended replica of the differential CCD array output signal, with most common-mode interference removed.

Track-and-Hold Amplifiers and Multiplexers

The Track-and-Hold Amplifiers and Multiplexers allow a single A/D Converter to digitize all the analog samples from all CCD arrays by time-multiplexing the output samples to the single converter. The eight Track-and-Hold circuits are identical; and, for brevity, only the CH 1—Side 1 circuitry will be described.

The GCX output from the A30 gain cell board (GC11) is applied directly to sampling switch U560A, an enhancement-mode MOS-FET device. The switch gate is controlled via Q660 by the $\overline{\text{OSAM1}}$ (Output Sample from Channel 1) logic signal, and is closed when the data being shifted out of the CCD is stable. When $\overline{\text{OSAM1}}$ is LO, the switch is on, and hold capacitor C774 charges to the signal level of GC11. When $\overline{\text{OSAM1}}$ is HI, the switch is off, and C774 holds its voltage level. Figure 3-3 (shown previously in the "System Clocks" description) shows the timing of $\overline{\text{OSAM1}}$ and $\overline{\text{OSAM2}}$ during the Slow-Out and Short-Pipe modes of CCD operation. During Fast-In mode, $\overline{\text{OSAM1}}$ and $\overline{\text{OSAM2}}$ are both held LO.

The level stored on Hold capacitor C774 is buffered by operational amplifier U770A. The operational amplifier, along with Q774, converts the applied input sample voltage to output current.

Selection of the CH 1—Side 1 current signal to be digitized by the A/D Converter is controlled by the $\overline{MS11}$ (Multiplexer Select-Channel 1—Side 1) line. As shown in Figure 3-3, only one of the eight MS signals will be LO at any time. A LO $\overline{MS11}$ signal applied to the base of Q773 will turn that transistor off. The other transistors of CH 1 (Q873, Q770 and Q870) and all of the CH 2 transistors (Q783, Q883, Q780 and Q880) are on to shunt their associated signal currents to ground. Each of the eight shunting transistors will be turned off in sequence to allow its associated signal current to pass to the CCD DATA node via a series common-base transistor (Q775 for Channel 1—Side 1). The resulting CCD DATA signal is a time-multiplexed combination of all eight CCD output channels (four from CH 1 and four from CH 2).

Precise current matching of the signal offsets for the four sides of Channel 1 is achieved by setting the DAC-generated CT11 (Center 11), CT12, CT13 and CT14 voltages at self-calibration. Similar offset matching for CH 2 is done with the CT21, CT22, CT23 and CT24 signals.

Secondary Supplies

The Secondary Supplies circuit, composed of U861A, U861B, U861C, U861D, and associated components, provides operating voltages used by the CCD Output circuitry. The voltage level of the A2D REF (−0.5 V analog-to-digital reference) is determined by the current through R861 from operational amplifier U861C and is set by the resistive divider string formed by R763 and R764 from the +10 VREF supply. The other voltage outputs (+8.5 V and +10 VRA and +10 VRB are set by the various taps on the resistive voltage divider and buffered by operational amplifiers.

A/D CONVERTER AND ACQUISITION LATCHES

The A/D Converter and Acquisition Latches (diagram 15) circuit consists of eight-bit A/D Converter U560, eight-bit Min-Max Comparator U740 and U732 (for ENVELOPE acquisitions), Acquisition Latches U631, U632, U630, and U640, and latch switching circuitry to direct and latch the acquired data point values.

A/D Converter

A/D Converter U560 is an 8-bit flash converter that digitized the analog samples from the CCD arrays at an overall conversion rate of 4 MHz.

The A2D REF voltage (—0.5 V) is amplified and inverted by U880 to produce the 1.5 V reference voltage used by the A/D Converter. Noise and ripple are filtered from the amplified reference voltage by L770, C570, and C776. The negative side of the reference is tied to ground; therefore, input voltage for conversion may range from 0 V to +1.5 V. The time-multiplexed CCD Data signal current develops a voltage across R880 that is offset by the A2D REF voltage. It is then amplified and inverted by U780 to produce an input signal to the A/D Converter within the 0 V to +1.5 V range needed. The amplified signal is applied to the analog input of U560 after being filtered by L780 and C770.

The input sample is converted on the falling edge of $\overline{SHIFT}$, a 4 MHz clock signal. A valid data byte representing the analog input voltage appears on the output of the A/D Converter approximately 20 ns later. That data byte is applied to the 8-bit Magnitude Comparator formed by U740 and U732, with the four LSBs going to U740 and the four MSBs of the byte going to U732.

Envelope Min-Max Comparator

For ENVELOPE Mode acquisitions, glitch-catching at the slow SEC/DIV settings is done by the Envelope Min-Max Comparator circuit formed by four-bit comparators U740 and U732. At SEC/DIV settings slower than 50 μs, analog Peak Detectors U440 and U340 provide more samples than needed to fill the required 50 data points (25 min-max pairs) per division, so not all are saved. During each envelope sampling interval (1/50 of the SEC/DIV setting at 50 μs and slower), the Min-Max Comparator compares every Peak Detector min/max value from A/D Converter U560 to the last-latched maximum or minimum byte to determine which sample will be saved. If the new byte value is greater than the latched byte value, the MAX output of Comparator U732 (pin 5) will go HI; if less than the latched value, MIN at pin 7 will go HI. If the A/D output value is equal to the latched value, both connected outputs of Magnitude Comparator U732 will remain LO. The final min byte and max byte obtained from each channel during an envelope sampling interval are saved to the Acquisition Memory as part of the envelope waveform record.

Since the input to the A/D Converter is time multiplexed between CH1 maximum, CH2 maximum, CH1 minimum, and CH2 minimum values from the Peak Detectors, the latched data applied to the Magnitude Comparator from the Max/Min Latches must also be time multiplexed to maintain the correct relationship for making the comparisons (CH 1 maximum against CH 1 maximum, CH 1 minimum against CH 1 minimum, etc.). The necessary time multiplexing is done by the Envelope Latching Logic circuitry.

Acquisition Latch Switching

NORMAL MODE ACQUISITIONS. In non-envelope mode, the LOAD LATCHES signal from the Time Base Controller remains in its HI state. With LOAD LATCHES HI at one of the inputs of OR-gates U512A and U512B, the MIN and MAX signals from the Envelope Min-Max Comparators are ignored, and the outputs from the gates are held HI. This causes each sample from the A/D Converter to be clocked directly through the Acquisition Latches.

Output enabling of the four Acquisition Latches is controlled by the MS13+MS11, MS12+MS14, MS23+MS21, and MS22+MS24 multiplexer select lines, which are logically ANDed combinations of the lines that control the multiplexing of the CCD analog samples to A/D Converter U560. The states of these select lines, only one of which may be HI at a time, are latched into the four flip-flops of U520 and U521 by the 20 MHz system clock (C20M1). The $\overline{Q}$ outputs of the flip-flops control output enabling of the four Acquisition Latches. One at a time, their outputs are enabled to apply the acquired data point to the output bus for transfer to the Acquisition Memory input buffer (U613, diagram 8). After one of the Acquisition Latches has been enabled for 100 ns, the rising edge of the CLKLATCH signal clocks the HI state present on the D inputs of the flip-flops of U510 and U511 to the Q output of the enabled flip-flop. That rising edge then clocks the data byte from the A/D Converter through the enabled Acquisition Latch to the input buffer of the Acquisition Memory.

ENVELOPE MODE ACQUISITIONS. In ENVELOPE MODE, the LOAD LATCHES signal input to U512A and U512B (from the Time Base Controller, diagram 8) forces each clock flip-flop in turn to clock the A/D Converter output data byte into its associated latch by holding their D inputs HI during the first four data point conversions in each envelope sampling interval. These first four samples (one byte in each Acquisition Latch) initialize the min/max data in the latches for comparison to the remaining data samples that occur in the envelope sampling interval.

The Acquisition Latch Switching circuitry multiplexes the latched CH 1 and CH 2 maximum and minimum data bytes to the inputs of the Envelope Min-Max Comparator so that each digitized sample from the A/D Converter is compared to the correct previous sample (CH 1 Min to the previous CH 1 Min, etc.). (Note—odd sides of the CCDs are minimums, even sides are maximums.) It also provides the proper enabling and clocking to direct a new maximum or minimum data bytes into the correct Acquisition Latch.

As in NORMAL Mode acquisitions, output enabling of the four latches is controlled by the MS13+MS11, MS12+MS14, MS23+MS21, and MS22+MS24 select lines. The $\overline{Q}$ outputs of the flip-flops control output enabling of the four latches, causing the Acquisition Latch corresponding with the selected CCD output (CH 1 or CH 2, maximum or minimum) to apply the previously latched data byte to the inputs of the Envelope Min-Max Comparator. A/D Converter output data is thus always being compared to the proper maximum or minimum data value.

When the Envelope Min-Max Comparator detects that the A/D Converter output byte value is either above or below the latched byte value, the MAX or MIN output of U732 will go HI respectively. The HI is passed through U512A (MIN) or U512B (MAX) to the D inputs of flip-flops U510 and U511. Since the A/D Converter output byte value could represent any of the four CCD array channels, the multiplexer select lines that determine what sample is currently being output from the CCD arrays are applied to the reset inputs of U510 (A and B) and U511 (A and B). Only that clocking flip-flop corresponding to the selected data sample is enabled by a HI data select line; all others remain in the RESET state.

When the CLKLATCH (4 MHz) clock occurs, the enabled clocking flip-flop transfers the level at its D input to its Q output, LAxMAX (latch CH × max). If that level is a HI (a new max has been found), the current A/D Converter output data byte (the new max) will be latched into the associated Max Latch (either U632 or U631, depending on whether it is CH 1 or CH 2 data), where it then becomes the new comparison level. MIN clocks are produced by U510B and U511A in a similar fashion, latching the new MIN values into either U640 or U630.

Acquisition Latches

During Envelope Mode, the Acquisition Latches perform as Min-Max latches (U631 and U632 Max; U630 and U640 Min) to hold the maximum and minimum data point values being compared during the sampling interval. These values are compared to each newly converted waveform sample to determine when new maximums or minimums occur. Output enabling and data latching are controlled by the Acquisition Latch Switching as previously described.

DISPLAY AND ATTRIBUTES MEMORY

The Display and Attributes Memory (diagram 16) is where the Waveform Processor stores waveform and readout data that is to be displayed on the crt. Digital-to-Analog converters (DAC), under control of the Display Control circuits, convert this stored data to the vertical- and horizontal-deflection signal currents that drive the Display Output amplifiers.

Vertical Display RAM

Vertical Display RAM U431 stores the vertical-deflection data for four 512-point waveforms. Data points to be displayed are written from the Save Memory into the RAM by the Waveform μP (diagram 2) on the WD bus (waveform data bus) via bus transceiver U322. The stored waveform display bytes are read sequentially out of the Vertical Display RAM in blocks under control of the Display Counter (diagram 17) and applied to Vertical DAC U142 to produce the analog vertical deflection signal of the displayed waveform.

To write data into the Vertical Display RAM, the Waveform μP puts the data byte to be written onto its WD bus and sets its $\overline{\text{WRD}}$ (waveform read) bit HI. This HI enables bus transceiver U322, and the vertical data is applied to I/O (in/out) pins of the RAM. At the same time, the $\overline{\text{DISP}}$ signal is address decoded LO (from decoder U570, diagram 2) for addresses between 8K and 12K, and the WAB address bit applied to U323B selects the Vertical RAM U431 via U421A. When the Waveform μP generates its write pulse ($\overline{\text{WWR}}$), it is transmitted through U422A and U422D, writing data into the Vertical Display RAM. This process occurs for each data byte (point) of waveform information.

To display the stored data points, the System μP loads the starting address of the data block to be displayed into the Display Counter and selects the Display Counter to address the Vertical Display RAM (via the Address Multiplexer). The System μP also sets the $\overline{\text{YON}}$ (vertical display on) bit applied to U421A and U421B LO, selecting the Vertical Display RAM and enabling its outputs. As the Display Counter increments, the selected block of data is sequentially clocked out onto the DY bus (vertical-display data bus) and applied to Vertical DAC U142 to produce the vertical deflection signal current to the Vertical Output Amplifiers.

If the Waveform μP needs to read data from the Vertical Display RAM, it outputs an address within 8K to 10K address space of the RAM. This address block is decoded by U323B to enable both the Vertical Display RAM (via U421A) and bus transceiver U322. Since the Waveform μP is trying to read data, its $\overline{\text{WRD}}$ (waveform processor read) line will be set LO. This enables the RAM outputs via U323C and U421B and causes buffer U322 to direct the data onto the Waveform μP data bus.

Horizontal Display RAM

Operation of Horizontal Display RAM U440 is identical to that of the Vertical Display RAM just described. The Horizontal RAM chip select ($\overline{\text{CSX}}$) is gated through U323D for addresses between 10K and 12K when $\overline{\text{DISP}}$ is LO.

Data that may be stored in the Horizontal Display RAM includes two 512-point waveforms and 1K $\times$ 8 of readout information. During a waveform display, the data output from the Horizontal RAM may be routed to either the Vertical DAC or Horizontal DAC, providing for either two more YT displays or two XY displays.

Attributes RAM

Attributes RAM U430 contains 4K $\times$ 1 points of data that tell the Z-Axis system (using the BRIGHTZ signal) whether or not a data point read from either the Vertical Display RAM or the Horizontal Display RAM should be intensified. Operation of the RAM is similar to that just described for the Vertical and Horizontal RAMs except that the data path is only one bit wide.

The write enable of the Attribute RAM ($\overline{\text{WRA}}$) is gated by U422C between 12K and 14K when $\overline{\text{DATT}}$ is LO from decoder U570 (diagram 17). $\overline{\text{WRA}}$ going LO enables the data from bit WD7 of the data bus to be written to the addressed location. Gate U422A prevents the $\overline{\text{WWR}}$ clock from being gated to U422C if the Display Counter is selected (Waveform μP not in control of the address bus).

To read attribute data out of the RAM, the Waveform μP sets $\overline{\text{WRD}}$ LO. This LO, along with the address-decoded $\overline{\text{DATT}}$ (attribute data) line, enables buffer U423A and places the addressed output bit from the D0 output of U430 onto bit WD7 of the data bus.

When displaying data from either (or both) the Vertical RAM or Horizontal RAM (the addresses applied to all three RAM chips are the same), the attribute data for each data point will be applied to the Z-Axis circuit to determine the intensity of each point. A HI bit from the D0 output of U430 will intensify the displayed point.

Horizontal Data Buffers

The Horizontal Data Buffers, U320 and U321, are used to route the data from the Horizontal RAM to either the Horizontal DAC or the Vertical DAC, depending on the type of display being produced.

For normal waveform displays, vertical deflection data may come from either the Vertical or the Horizontal Display RAM. To route data from the Horizontal RAM to the Vertical DAC, the outputs of the Vertical RAM will be disabled ($\overline{\text{OEY}}$), the outputs of the Horizontal RAM will be enabled ($\overline{\text{OEX}}$ goes LO), and buffer U320 will be enabled ($\overline{\text{XTOVERT}}$ goes LO). These three signals are all controlled by the System μP by writing bits XON and XTOVERT HI into Mode Control Register U541 (diagram 17)

and writing a LO to the YON output of the register. Now, data addressed in the Horizontal RAM is applied to the Vertical DAC to produce vertical waveform deflections.

For XY displays, Mode-Control bits XON, YON, and XY are set HI while XTOVERT is set LO. This applies addressed data from the Vertical RAM to the Vertical DAC and applies the addressed data from the Horizontal RAM to the Horizontal DAC via now-enabled buffer U321. A waveform versus waveform (XY) display results.

During readout displays, both U320 and U321 will be disabled, along with the Vertical RAM. Since the readout character-code data is stored in the Horizontal RAM, it will be enabled. Character-code data from the Horizontal RAM is output to the Readout State Machine, where it is converted to the appropriate horizontal- and vertical-deflection codes.

Readout Buffers

Readout buffers U240 and U140 direct the ten least significant bits (LSB) from the Display Counter to the Horizontal DAC and the Vertical DAC during readout displays. The buffers are enabled by a LO $\overline{RO}$ signal at their enable inputs.

Four of these bits, Q6-Q9, are applied to the four most significant bits (MSB) of the Vertical DAC input through U140A and are used to select one of the 16 available readout lines for the selected character to be displayed on.

The six LSBs are applied to the six MSBs of the Horizontal DAC and are used to select one of the 64 possible character positions on the selected readout line. Since a maximum of only 40 characters will actually be displayed on any given line, the gain of the Horizontal Output Amplifier increases when readout is being displayed. The center 40 character positions then fill the display horizontally. This action is more fully explained in the Horizontal Output Amplifier description.

Ramp Buffers

Ramp Buffers U130 and U140 apply the ten LSBs of the Display Counter address (via Address Multiplexer U210, U212, and U221 on diagram 17) to the Horizontal DAC during YT waveform (non-XY) displays. Since the Display Counter address is merely incrementing for waveform displays, a horizontal ramp results at the Horizontal DAC outputs. Each sequentially acquired data point is thus displayed at its corresponding horizontal (time-dependent) address on the crt. The buffers are enabled by the $\overline{COUNTEN}$ (counter enable) bit from the Mode-Control Register.

Volts Cursor Register

Volts Cursor Register U241 is an address-decoded memory location where the System μP writes the eight MSBs of the vertical-position data for volts-cursor displays. Data written into this register, along with two bits written into the Misc Register U540, define the vertical position of the Volts cursor. Since volts-cursor displays have two cursors, the microprocessor alternately writes the position data for each cursor into the registers just before it is displayed. Data is written into the register on the rising edge of the address-decoded $\overline{VCURS}$ clock pulse.

Volts-cursor displays are a special type of "waveform" display wherein the vertical deflection data from the Vertical Display RAM is disabled (by turning off the RAM chip select), and the data bits in Volts Cursor Register U241 (and the DY0-DY1 bits from the Misc Register U540, diagram 17) are applied to Vertical DAC U142 instead. Cursor display is automatically selected by the Z-Axis logic when neither WFM nor $\overline{RO}$ are asserted (not a waveform display and not a readout display). To start the display, the System μP asserts the START bit in the Display Control Register as it would for a waveform display, starting the Display State Machine. The result is a horizontal line displayed on the screen at the level set by the data from the Volts Cursor Register. When displaying cursors on a waveform, the two LSBs from the Misc Register are set to 0, decreasing the resolution from 1024 levels to 256 levels.

Time Cursor Register

Time Cursor Register U441 provides a function similar to the Volts Cursor Register. Time-cursor data is written to the register from the system processor on the rising edge of the address-decoded $\overline{TCURS}$ clock (time-cursor clock). This data is applied to Horizontal DAC U250 (along with the DX0-DX1 bits from the Misc Register) to define the horizontal position of the cursor. A software ramp previously written into Vertical RAM U431 is applied to Vertical DAC U142 as the Display State Machine runs (started in the same way as the volts-cursor display).

For "directed-beam" cursors, such as the "+" made up of individual microprocessor-directed points displayed on screen, both cursor registers are enabled after the System μP writes one dot of XY position data into the registers. To display the addressed point, the processor sets the HZON (host z-axis on) bit in the Misc Register LO, then HI. The processor then calculates the next point of the "+", writes the position data to the cursor registers, enables the registers, and sets $\overline{HZON}$ LO to display that point. This cycle continues until the entire "+" is drawn.

Vertical DAC

Vertical DAC U142 generates complementary vertical-deflection currents used to drive the vertical deflection system from the digital data applied to its inputs. The data that appears at the DAC inputs is selected by the microprocessor via the Mode-Control Register and determines what type of display will be generated. The exclusive-OR gate U350A inverts bit DY9 during "non-readout" displays to create "bipolar" data relative to the vertical (graticule) center of the crt.

Horizontal DAC

Operation of Horizontal DAC U250 is identical to that of the Vertical DAC and produces the horizontal-deflection signal currents that drive the Horizontal Output Amplifier.

Diagnostic Buffers

The Diagnostic Buffers, U141 (vertical) and U243 (horizontal), allow the System μP to monitor the data being applied to the Vertical DAC and Horizontal DAC respectively. By forcing known data patterns through the various data paths and observing the data arriving at the DAC inputs, the diagnostic routines can verify functionality of much of the display system hardware. The buffers are enabled during diagnostics via the address-decoded Register Select logic.

DISPLAY CONTROL

The Display Control System (diagram 17) produces the crt waveform and readout displays from data stored in the Display RAM. The data, originally stored by the Waveform μP or the System μP, is read out of the RAM and is used to produce the individual dots that make up both waveform and readout displays. The Display System has two "state machines" for converting the stored data into the horizontal and vertical deflections that produce the waveform dots and readout characters.

For YT waveform displays, the Display State Machine generates 512 linearly spaced points across the face of the crt (horizontally). Each of these points may be displayed at any of 256 vertical positions on the crt. For XY displays, each of the 512 points that make up a waveform may be placed anywhere on the screen in a 256 × 256 matrix.

For readout displays, the face of the crt is vertically divided into 16 character lines each having 40 horizontal character positions on the line. Each of these character positions corresponds to a specific location in the readout memory space (stored in the Horizontal RAM). To display the readout, the Readout State Machine sequentially reads through the readout memory and displays the required character at the corresponding (memory-mapped) location on the crt screen. Each displayed character consists of a sequence of individual dots produced by the Readout State Machine.

Each of these display types is controlled and initiated by the System μP. The acquired waveform data points are written into the Display RAMs by the Waveform μP and the readout data is written in by the System μP. Display of this stored data is controlled by the System μP through data latched into the several display registers. The data written to the registers determines what type of display should be produced, how long (number of data points) it should be, and when it should start.

Register Select

The Register Select stage, composed of U550 and U450D (along with the System μP address decoding), address decodes the three LSBs of the System μP address bus to enable any of eight display "registers" for a read or write. These registers control such things as display mode (how the stored data is displayed, either XY or YT), which waveforms are displayed, and whether or not cursors and readout are to be displayed.

The enable inputs for U550 are controlled by the System μP. The $\overline{\text{DISPSEL}}$ (display select) is an address-decoded signal produced on the Processor board when any of the display memory addresses are output by the System μP. Negative OR gate U450D provides an enable to $\overline{\text{U550}}$ whenever the System μP is trying to read or write. Address bit A3 provides the final enable when it is HI.

Once enabled, the three lowest address bits are used to select one of the eight outputs from U550. These outputs, when LO, enable or load one of the eight display registers. Enabling of these individual registers is explained in more detail in the specific register descriptions.

Mode Control Register

Mode Control Register U541 and associated gating circuits composed of U340, U442, U423B, and U350C, control the operating modes of the various display state machines.

Data from the processor data bus is written into data latch U541 when the $\overline{\text{MODECON}}$ (mode control) bit from U550 returns HI (after the PWRUP reset goes HI). These

latched bits are used as enables to other portions of the display circuitry and control the overall function of the display.

NAND gates U340C and U340D do not allow the $\overline{YON}$ and $\overline{XON}$ enables (controlling the vertical and horizontal RAMs respectively) unless the display counter is running (PRESTART + DISPLAY is HI). Exclusive-OR gate U350C and tristate buffer U423B are used to enable horizontal-deflection bit DX1 only when the time cursor is being displayed (both RO and COUNTEN are LO). The remaining bits from the mode-control register are NANDed with the $\overline{DISP}$ (display running) signal and only affect their associated functions while the Display State Machine is running.

Buffer U542 provides a way for the System μP to read back the data written to the Mode Control Register U541.

Display Control Register

The operation of Display Control Register U530 is similar to that just described for the Mode Control Register. When enabled (by $\overline{DISCON}$), data from the data bus is written into U530 on the rising edge of the System μP $\overline{WR}$ (write) clock. These data bits determine how many data points are displayed, whether the display is to be read from memory in envelope mode (ENV), and whether the intensity of each dot should be bright or dim (DOTS).

The buffer U531 provides a way for the System μP to read back the contents of the Display Control Register.

Miscellaneous Register

Operation of the Miscellaneous Register is identical to that of the Display Control Register just described. The output bits control miscellaneous circuit functions, as the register name implies. The function of each bit is explained in the description of the associated circuitry.

Buffer U540 allows the System μP to read back the contents of the Miscellaneous Register.

Display Clocks

The state machines of the Display System run on clocks derived from the 5 MHz clock of the Secondary Clock Generator U710 (diagram 7). The Display Clocks circuit provides the signal frequency division and gating logic to properly condition clocks for the Display System circuitry.

The 5 MHz clock signal from the Time Base Controller circuit is buffered and inverted by U413C and is used to drive the Readout State Machine.

The 5 MHz clock is also applied to the counter made up of decade counters U410A and U410B, producing several intermediate clocks at their outputs. The 1 MHz 2QC clock, the 500 kHz 2QA clock, and the 250 kHz clock from U410B are gated together by U411A and produce the $\overline{SAMPLE}$ clock, having a LO duty cycle of 12.5%.

Buffer U413A inverts the 250 kHz clock used for the Z-Axis and Display State Machines.

Gates U411C, U412C, and U412D make up a clock-steering circuit that selects the source for clocks to the counters, depending on display mode. When displaying waveforms, readout, or cursors, the DISPLAY bit applied to U411C is HI. The RO and $\overline{RO}$ signals, applied to U412C and U412D respectively, do clock selection depending on whether readout or waveform data is to be displayed.

For waveform displays, RO applied to U412C is LO, holding its output to U411C HI. This HI, along with the HI DISPLAY bit, enables U411C, and the output of U411C follows the 250 kHz signal applied to U412D (since $\overline{RO}$ is HI). For readout displays, RO and $\overline{RO}$ are HI and LO respectively. This holds the output of U412D HI, and the output of U411C follows the $\overline{CLKRAM}$ (clock RAM) signal from the Readout State Machine. To completely disable the Counter clocks, the Display State Machine sets the DISPLAY bit applied to U411C LO.

Display Counter

The Display Counter stage, made up of U211, U220, and U222, generates the sequential addressing that the Display and Readout State Machines use to read the stored waveform and character data out of the display RAM. Depending on the type of information to be read from RAM (waveform or readout), clocks to the counter are selected by logic to produce waveform and readout displays at the proper refresh rates.

To display stored data, the System μP writes the eight MSBs of the 12-bit starting RAM address into U211 and U220 over the data bus by generating a LO $\overline{LDCOUNT}$ from the Register Select stage. The 4 LSBs of the address (all LO) are also loaded at the same time into U222. The counter then starts counting at the selected rate. When the count in U222 reaches 15, its $\overline{RCO}$ (ripple-carry output) goes LO for the last half of the clock cycle and

enables U220. Due to a two-gate propagation delay through U222 to the $\overline{RCO}$ output, U220 will still be enabled on the rising edge of the next clock. This clocks U220, which is then disabled until U222 counts another 16 clocks. Counting continues, and eventually the $\overline{RCO}$ output of U220 enables U211, causing it to increment in a similar fashion. Counting continues until the Display State Machine determines that the desired display is complete, at which time it shuts off clocks to the counter.

The outputs of the counters change synchronously and are applied to the Multiplexer stage, which selects between these counter outputs and the microprocessor address bus for Display RAM addresses. The MAX output from U222 (occurring on count 15) is used in the Readout State Machine.

Address Multiplexer

The Address Multiplexer stage, under control of the Display State Machine, selects the address source for the various display RAMs from either the Waveform μP address bus or the Display Counter.

When the Waveform μP is writing acquired data into the display RAMs (Horizontal or Vertical), the Display State Machine selects the Waveform μP address bus (WA0-WAB) as the source for RAM addresses by setting the COUNTSEL (counter select) line LO. When displaying the stored data, COUNTSEL is HI, and the outputs from the Display Counter are routed to the various RAM address lines.

Exclusive-OR gate U350B is used to invert counter bit DC0 when displaying envelope data (ENV is HI). This causes data pairs (max-min) to be read out in reverse (relative to how they were stored) and produces an envelope display that always starts with a MIN point.

Display State Machine

The Display State Machine determines when display of stored data should start and stop, depending on other conditions in the Display System.

To start a display, the System μP writes a HI for the START bit into Display Control Register U530. This HI is applied to the D input of flip-flop U415A and clocked to its Q output on the falling edge of the 250 kHz clock (rising edge of the $\overline{250\ kHz}$ clock). This latched STARTDIS bit (HI) is then applied to the D input of U414A and to pin 9 of U313. Since the Display Counter has not reached its final value (this is the starting point), the output level of the three lower AND gates within U313 are LO, thereby enabling the output AND gate (it has inverting inputs). With the previous display cycle finished (as it is for this discussion), the DISDN (display done) bit applied to pin 10 of U313 is also HI. The 250 kHz clock applied to this enabled AND gate causes the output of U313 to go HI on the falling edge to clock the HI STARTDIS bit to the Q output of U414A. This latched signal is the DISPLAY bit that enables the Display Counter clocks (via U411C).

The DISPLAY bit is delayed slightly by the propagation delays of the START bit through the flip-flops and gates. Therefore, the PRESTART bit is written HI to cause the output of U323A to be HI until the DISPLAY bit is latched into flip-flop U414A. The HI PRESTART + DISPLAY bit from U323A selects the counter outputs to address the Display RAMs (via the Address Multiplexer stage). After the DISPLAY bit is latched into U414A, the System μP sets the START and PRESTART bits from the Display Control Register LO. The LO START bit is clocked to the Q output of U415A, disabling the 250 kHz clocks through U313 to U414A, and the LO PRESTART bit allows the DISPLAY signal to control OR-gate U323A.

With the DISPLAY bit to U411C set HI, clocks from either U412C or U412D clock the Display Counter. Which one does the clocking depends on whether the data to be displayed is readout or waveform information. If readout information is being displayed, the $\overline{RO}$ bit (from the Mode Control Register) applied to U412D will be LO, disabling the 250 kHz clock (output of U412D is held HI). At the same time, R/O applied to U412C is HI, enabling the $\overline{CLKRAM}$ (clock RAM) signal from the Readout State Machine to clock the address counters.

If waveform data is to be displayed, $\overline{RO}$ from the Mode Control Register is HI and RO is LO. The LO RO level applied to U412C closes the $\overline{CLKRAM}$ path (output of U412C is held HI) while the HI $\overline{RO}$ level applied to U412D opens the 250 kHz clock path through U412D and U411C.

The two display-control bits, STOP512 and STOP1024, applied to U313 determine how many data bytes are read from the selected display RAM (Horizontal, Vertical, and Attribute) before stopping the current display cycle. Only one of these two bits is HI at any time. The outputs of the unselected AND gates within U313 are LO, and along with the LO caused by the LO STARTDIS bit, enable the output gate of U313. The selected AND gate watches its appropriate counter bit and, on the falling edge of the bit, causes a clock at the output of U313. This clocks the now LO STARTDIS bit to the Q output of U414A, disabling U411C (and thus clocks to the Display Counter), and resets the DISDN at the $\overline{Q}$ output HI in preparation for the next display cycle.

The DISDN signal is also sent to the System μP Interrupt Logic to tell it when the currently assigned display task is complete. When the processor detects the HI DISDN, it writes data out to the display register to start the next display cycle. The System μP, knowing how much waveform and readout data needs to be displayed, does the writing at a rate that keeps the overall display-refresh rate constant.

Displaying a single waveform requires 512 data points be read from RAM, so STOP512 is set HI. A two-waveform display or a single-waveform envelope display will require STOP1024 to be HI. Readout displays may also consist of up to 16 lines of readout, in which case STOP1024 would be set. This is further explained in the Readout State Machine description.

The $\overline{\text{STOPDIS}}$ bit applied to the reset inputs of U414A and U415A provides the System μP with a way to stop any display in process.

Z-Axis Logic

The Z-Axis Logic determines when to turn the display beam on or off for each of the various display modes. These displays are readout, waveform, cursor-normal, cursor-dashed, and diagnostic (host-forced) Z-Axis on.

To enable readout or waveform displays, the Display State Machine sets its DISPLAY output HI. This enables U415B, U414B, and U312C.

During readout displays, the $\overline{\text{RZON}}$ (readout Z-Axis on) signal from the Readout State Machine is LO for each point that should be turned on and HI when the display should be blanked. The level of this signal is sampled by U415B at a 5 MHz rate. The Q output of U415B controls the Z-Axis through U450B and U223C, and since it is synchronized to the 5 MHz clock used to clock the Readout State Machine, the intensity of each dot is not the same.

For waveform displays, the DOTS bit from Display Control Register U530 will be set HI by the System μP. This HI, along with the HI DISPLAY signal from the Display State Machine, enables U312C. As long as a waveform display is taking place, the 250 kHz clock turns the display dots on and off with a 50% duty cycle via U312C and U223C. When the Display State Machine determines that the waveform display is over, it sets its DISPLAY bit LO, disabling U312C. For nonwaveform displays, the DOTS bit is LO, also disabling U312C.

For cursor displays, the HI DISPLAY signal enables D flip-flop U414B, and the $\overline{\text{250 kHz}}$ clock begins clocking the data from the output of U312B to the Q output of U414B. Since a cursor display is neither a waveform nor a readout display, the DOTS signal applied to inverter U413D is LO while the $\overline{\text{RO}}$ signal applied to NAND-gate U312B is HI. This enables U312B, and the output of U412A then controls the D input signal to flip-flop U414B. That signal is clocked to the Q output and applied to U223C to control the Z-Axis signal $\overline{\text{ZON}}$.

When displaying the inactive cursor (the one not selected for control by the cursor pot), the ACTIVELC (active line cursor) bit from the Misc Register to pin 2 of U412A is set LO. This causes the output of U412A to be HI, and the Z-Axis remains on as long as that particular cursor is being displayed.

When the other (active) cursor is to be displayed, the System μP sets the ACTIVELC bit HI. The output of U412A is then dependent on the DC3 signal from the Display Counter. The DC3 signal has a 50% duty cycle and changes states every eight characters (for cursors, the character is a single dot), so the resultant cursor display appears as a dashed line.

The $\overline{\text{HZON}}$ (host Z-Axis on) bit applied to U450B from the Misc Register (U540) allows the System μP to turn the Z-Axis on during diagnostics and allows verification of Z-Axis functionality. When set LO, $\overline{\text{HZON}}$ produces a LO at the output of U450B output, and thus at the $\overline{\text{ZON}}$ (Z-Axis on) output of U223C. This keeps the Z-Axis turned on until the $\overline{\text{HZON}}$ bit is reset HI by the processor.

Readout State Machine

The Readout State Machine produces the alphanumeric readout on the crt from character-code data stored in the Horizontal RAM. For readout displays, the face of the crt is vertically divided into 16 character lines each having 40 horizontal character positions on the line. Each of these character positions corresponds to a specific location in the readout memory space (stored in the Horizontal RAM). To display the readout, the Readout State Machine sequentially reads through the readout memory and displays the required character at the corresponding (memory-mapped) location on the crt screen. Each displayed character consists of a sequence of individual dots produced by the Readout State Machine.

Since the position of the character on the screen is related directly to the RAM location, the LSBs of the Display Counter are used to position the character on the crt screen. The six LSBs of the counter are applied to the Horizontal DAC and select 1-of-64 character locations on

a line (only the center 40 are displayed) and the next four LSBs are applied to the Vertical DAC to select 1-of-16 display lines.

Once this rough positioning is done, the Readout State Machine displays a sequence of dots that make up the addressed character, each dot being positioned relative to the rough display position.

Character codes, sequentially read from the Horizontal RAM, are applied to seven address lines of a character ROM (U420). These select the block of dot-position data within the ROM corresponding to that character code. Five more address bits are generated by an incrementing Dot Counter (U416B and U416A) and sequentially clock the XY dot-position data from the selected ROM block. The horizontal and vertical dot-position data is applied to the Horizontal and Vertical DACs and is used to deflect the crt beam relative to the selected on-screen character position.

The operation of the Readout State Machine is ROM based; it proceeds through a sequence of states based on data loaded from a ROM.

Initially, when power is first applied, both the PWRUP (power up) and DISPLAY signals applied to U450A are LO. These states cause a LO at the reset input of presettable counter U231 that resets its output count to zero. The reset state will remain until the instrument power comes up (PWRUP goes HI) and the system processor determines that a display should be produced (it starts the Display State Machine and DISPLAY goes HI).

With the reset removed, presettable counter U231 is enabled to either count (up) or do a parallel load from the four MSBs output from the addressed location within U232 on the next rising edge of the $\overline{5\ MHz}$ clock. The COUNT/$\overline{LOAD}$ select line from the data selector U230 determines whether counting or loading will occur.

The LOAD/$\overline{DECIDE}$ bit output from the addressed ROM location within U232 is applied to the enable input of U230 and determines whether the COUNT/$\overline{LOAD}$ line is forced LO (U230 disabled by LOAD/$\overline{DECIDE}$ being HI) or whether one of the decision inputs is selected (via select inputs A, B and C of U230). When the LOAD/$\overline{DECIDE}$ bit from U232 is LO, it indicates that the state machine is at a decision point as to whether counter U231 should count or load (instead of just automatically loading the next state). The condition tested to make this decision is selected by the select inputs to U230 and are as follows:

D0—R/O (readout) goes HI when a readout display should start.

D2—AND gate U233A watches for the 12th character address (11).

D3—$\overline{EOCH}$ (end of character) goes LO on the last character dot and causes the next state to be loaded.

D4—EOL (end of line—X9 bit U440, diagram 16) goes HI when readout line is over.

D5—AND gate U223B watches for the 64th character address (63) to indicate that the next character is the beginning of a new line.

ROM U330, addressed in parallel with U232, outputs three bits unique to the state selected and is used to clock the dot counter (U416B and U416A), clock the Display Counter, and to turn on the Z-Axis for readout dots.

The flow chart in Figure 3-8 illustrates operation of the Readout State Machine.

As the state machine runs, the counter outputs of U231 (the "current-state") are first reset to state "0." The data output from the O4-O7 (outputs 4-7) lines of U232 contain the "next-state" data, O1-O3 (outputs 1-3) hold the select data for the data selector U230, and output O0 (output 0) is the LOAD/$\overline{DECIDE}$ bit. In addition, the outputs from U330, used to turn on the Z-Axis if appropriate ($\overline{RZON}$), increment the character ROM dot counter U416B-U416A ($\overline{CKDOTCTC}$), and clock the Display Counter ($\overline{CLKRAM}$) to address the next character, are now at their state 0 condition (all HI).

The COUNT/$\overline{LOAD}$ signal from U232 determines what action counter U231 takes when the next $\overline{5\ MHz}$ clock occurs. If LO, the data from outputs O4-O7 of U232 is loaded to the counter outputs; if HI, the counter increments.

The LOAD/$\overline{DECIDE}$ line, along with the three channel-select inputs to U230, gives the state machine the ability to determine when certain events have occurred. When the LOAD/$\overline{DECIDE}$ bit from ROM U232 is HI, indicating that no decisions need be made in the present state, data selector U230 is disabled and the COUNT/$\overline{LOAD}$ output to U231 are forced LO. On the next $\overline{5\ MHz}$ clock, the "next-state" data from U232 (outputs O4-O7) is merely loaded into counter U231.

If the "present-state" data output from U232 has the LOAD/$\overline{DECIDE}$ bit set LO, indicating that some circuit condition needs to be tested to determine what to do next,

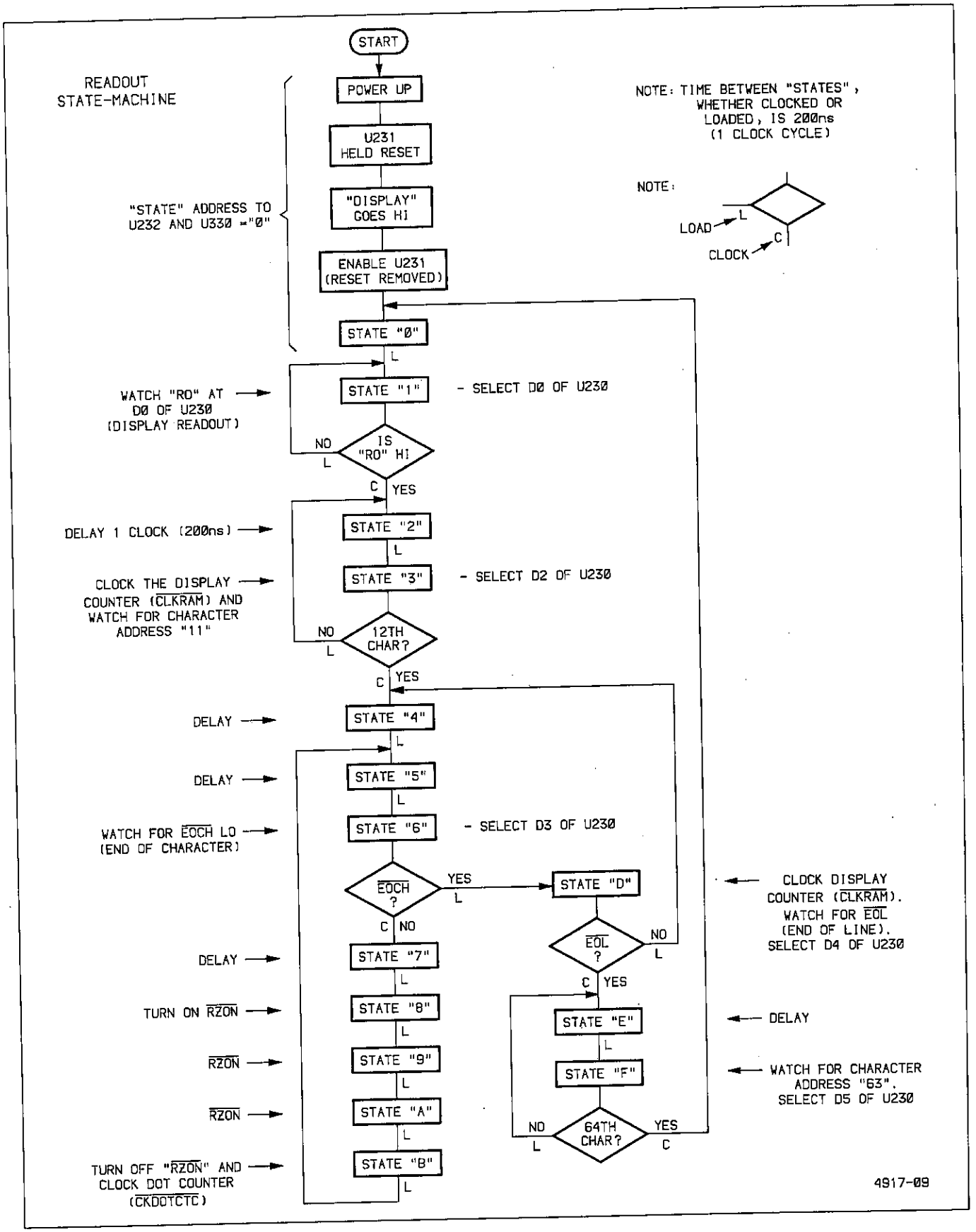


Figure 3-8. Readout State Machine flow chart.

data selector U230 is enabled. The three data bits (O1 through 03) from U232 define which condition needs to be tested and selects one of the D inputs of U230 to route to U231 via the COUNT/$\overline{\text{LOAD}}$ line. Whether or not the condition being tested for is present at the selected D input determines whether counter U231 counts or loads.

To go from state "0" to state "1," data from U232 is loaded into U231.

The state 1 data from U232 has the LOAD/$\overline{\text{DECIDE}}$ signal set LO, and the next three bits select input D0 of U230 to watch. This is the R/O (readout) line, and it is set HI by the System μP when it wants to start a readout display. If R/O is LO (don't start yet), COUNT/$\overline{\text{LOAD}}$ is also LO and the "next-state" data from U232 is loaded into counter U231. For state 1, the next-state data is also 1, so the state machine just cycles in state 1 until R/O goes HI.

When R/O goes HI, the COUNT/$\overline{\text{LOAD}}$ line follows and the next $\overline{5\text{ MHz}}$ clock increments the counter to state "2." State 2 has the LOAD/$\overline{\text{DECIDE}}$ bit set HI, so the next clock merely loads the next-state data (which happens to be 3) into U231.

State "3" clocks the display RAM (using $\overline{\text{CLKRAM}}$ from U330), enables U230, and selects its D2 input. AND gate U223A, producing the D2 input level, monitors the Display Counter address lines, looking for address 11. Address 11 corresponds to the twelfth character (remember character 0) and the first character displayed on the crt. (See Display Output description for further explanation.) If address 11 has not been encountered yet, the next-state data from U232 will be loaded into U231.

This next-state data is 2. Returning to state 2 resets the $\overline{\text{CLKRAM}}$ bit from U330 HI so the next state 3 will clock the Display Counter again. This loop between states 2 and 3 continues to clock the Display Counter until U223A detects address 11. When this occurs, COUNT/$\overline{\text{LOAD}}$ goes HI and the next $\overline{5\text{ MHz}}$ clock increments the state to "4."

State "4" resets $\overline{\text{CLKRAM}}$ HI and disables U230. The next clock loads state "5," a 200 ns delay, into U231. The next clock loads state "6."

State "6" data from U232 enables U230 and selects its D3 input. This is the $\overline{\text{EOCH}}$ (end of character) bit from the character ROM U420 and will only be LO for the last dot of any given character. As long as $\overline{\text{EOCH}}$ is HI (not the last dot), U231 will increment to state "7" on the next clock. State 7 disables U230, terminating the test condition.

State "8" is loaded from state 7 and turns on the Z-Axis via $\overline{\text{RZON}}$ (readout Z-Axis on) from U330. States "9" and "A" (hex) are sequentially loaded from the previous state and also have $\overline{\text{RZON}}$ asserted. These three cycles in sequence turn the Z-Axis on for 600 ns for each readout dot to be displayed.

State "B" is loaded from state "A" and does two things. It turns $\overline{\text{RZON}}$ off (HI) and sets $\overline{\text{CKDOTCTC}}$ (clock dot counter) LO, incrementing the dot counter made up of U416B and U416A. This addresses the next byte of XY deflection data within U420 in preparation for the next dot display cycle.

The next $\overline{5\text{ MHz}}$ clock loads state 5 from state B and resets the $\overline{\text{CKDOTCTC}}$ from U330 HI. State 6 is next loaded from state 5 and is once again checking for $\overline{\text{EOCH}}$ (described earlier).

If $\overline{\text{EOCH}}$ is set LO this time (signaling the last dot), counter U231 will be loaded to state "D" (instead of clocked to state 7 as described earlier). State D clocks the Display Counter via $\overline{\text{CLKRAM}}$, enables U230 and selects its D4 input. This input monitors the EOL signal (X9 bit) from the Horizontal RAM which will be set HI when the last character of a given line of readout information has been displayed. When EOL (end of line) is detected, U231 increments to state "E." If it is not detected, state 4 will be reloaded from state D data and the next character will be displayed as described before.

State "E" resets the $\overline{\text{CLKRAM}}$ signal from U330 and disables U230. The next $\overline{5\text{ MHz}}$ clock loads state "F" from state E data.

State "F" data clocks the Display Counter via $\overline{\text{CLKRAM}}$, enables U230 and selects its D5 input. AND gate U223B watches for Display Counter address 63; i.e., the 64th character. If the 64th character is not detected, state E is loaded from the state F data, resetting $\overline{\text{CLKRAM}}$ HI in preparation for the next state F and the associated $\overline{\text{CLKRAM}}$ pulse. The looping between states E and F continues to increment the Display Counter until U223B detects address 63 (the 64th character).

The 64th character is significant in that the next character is the start of the next line. When address 63 is detected, U231 is clocked from state F to state 0. The routine is now back to where it started, and the next line may be displayed in a similar manner.

DISPLAY OUTPUT

The Display Output circuits (diagram 18) convert the current outputs from the Horizontal and Vertical digital-to-analog converters (DACs) to the voltage levels used to drive the crt deflection plates. The Display Output circuit includes a vector-generation function that allows the individual dots of a waveform display to be translated into smooth lines connecting the waveform points (vectors on). A Display Mode switching circuit under control of the System μP selects which type of signal is applied to the output amplifiers for the various display types (envelope, dots, vectors, or readout).

Vertical and Horizontal Input Buffers

Operation of the Vertical and Horizontal Input Buffers is identical; so for brevity, only the Vertical Input Buffer circuit operation is described.

The Vertical Input Buffer, JFET operational amplifier U170 and its associated components, translates the complementary output currents from the Vertical DAC (U142, diagram 16) to an output voltage. Complementary, in this case, means that the sum of the currents is a fixed value; if one current increases, the other decreases by the same amount.

Current from the Vertical DAC output connected to pin 3 of U170 develops a voltage across R163. This voltage causes the output of U170 to move in the same direction until the feedback current through R164 applies an equal voltage to pin 2 of U170. The output voltage of the Input Buffer at pin 6 is the (signed) sum of voltages across R163 (+) and R164 (−). The gain of the stage is 1 V per mA (differential).

Vertical and Horizontal Vector Generators

Operation of the Vertical and Horizontal Vector Generators is similar. For brevity, only the Vertical Vector Generator is described in detail, and the differences in the two Vector Generators pointed out. Each Vector Generator consists of a High-Current Difference Amplifier, a Sample-and-Hold circuit, and an Integrator circuit that transforms the step voltages output from the Sample-and-Hold circuit to smooth transitions (vectors). See Figure 3-9 for a simplified diagram.

The step transitions from Vertical Input Buffer U170 are applied to the High-Current Difference Amplifier, made up of U281, Q182, Q181, and associated components, through R172. Initially (before the first integration occurs), input pin 3 of U281 is referenced to ground through R161; deviation from this ground reference seen at the other

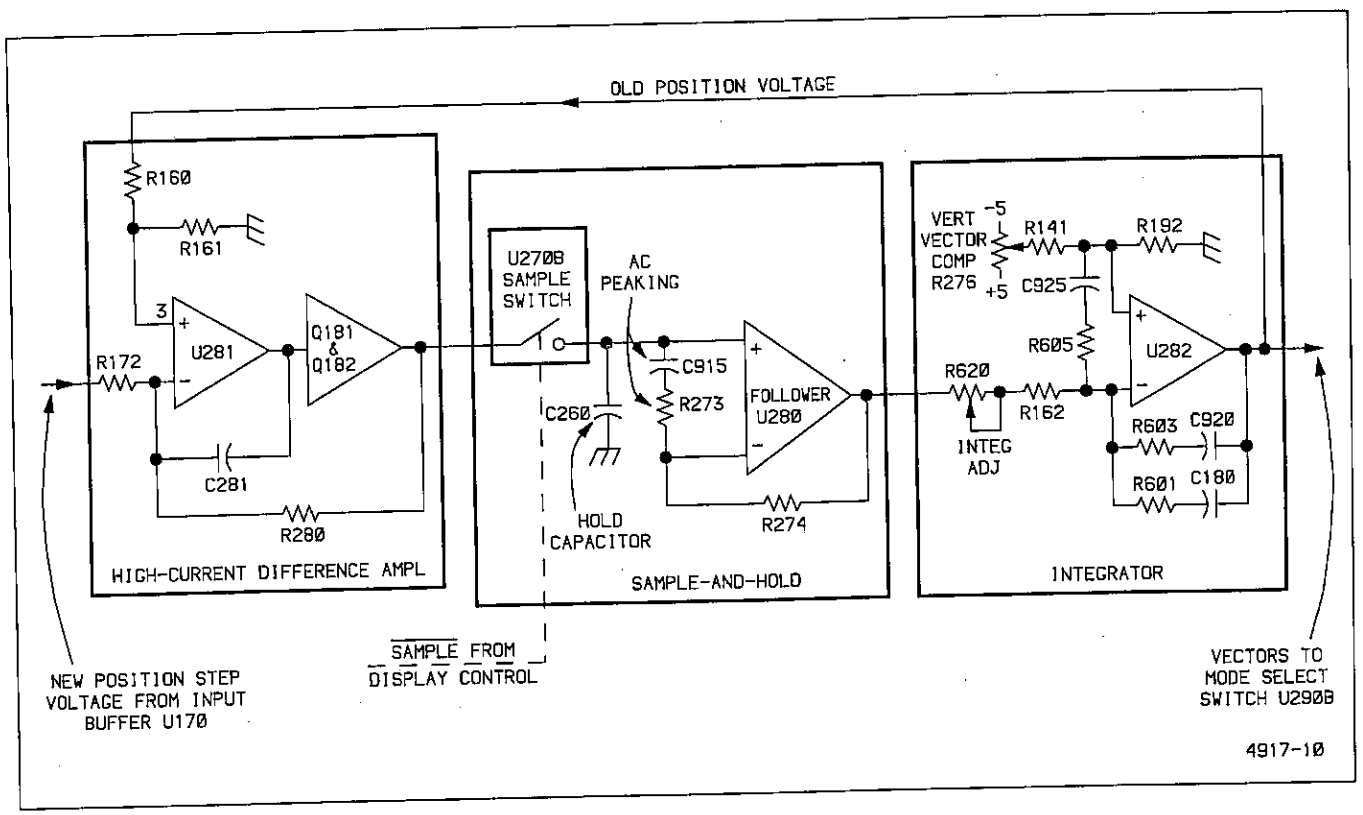


Figure 3-9. Vertical Vector Generator.

input (pin 2) causes the output (pin 6) of U281 to move in the opposite direction. This voltage change is applied to the base of Q181 (via R145) and to the base of Q182 (via series diodes CR193 and CR194 from R145). These transistors are biased in their linear region and act as emitter followers for the signals at their bases. Two series diodes between the bases of the transistors separate the base voltages by 1.2 volts, so the emitters of both transistors are at about the same potential. Negative feedback from the amplifier output (junction of R194-R196) is via R280. The resistance ratio of R280 to R172 sets the voltage gain of the amplifier at −1. Capacitor C281, from the output of U281 back to the input at R172, provides a fast feedback path to smooth transition spikes.

Sample Switch U270B, Hold Capacitor C260, and Voltage Follower U280 form a sample-and-hold circuit. The output of the High-Current Difference Amplifier at the junction of R194 and R196 is allowed enough time to settle to its new level before the 250 kHz $\overline{\text{SAMPLE}}$ pulse goes LO. At that time, the output of the Difference Amplifier is applied to the input of Voltage Follower U280A, and C260 is charged rapidly to that output voltage level. The $\overline{\text{SAMPLE}}$ pulse returns HI, and the BX output of the data selector goes to its high-impedance state to start the hold time. Voltage Follower U280 has high-impedance FET inputs; therefore, Hold Capacitor C260 discharges very little during the hold time.

The output of Voltage Follower U280 is held at the voltage level across C260; that level causes some value of current to flow through the series combination of R620 and R162 to the input of Integrator U282 (pin 2, the inverting input). The output of Integrator U282 at pin 6 ramps linearly for the duration of the hold cycle. (Actually, it ramps for almost the whole cycle, since the charge on Hold Capacitor C260 reaches the final level slightly before the sample switch is opened to start the hold time.) The time constants of the integrating network composed of R162 and of the series combination of R601 and C180 in parallel with R603 and C470 are such that the output of Integrator U282 reaches the new point position just as the next $\overline{\text{SAMPLE}}$ gate to U270B occurs. (A step change of 1 volt at the input causes a ramp of −1/4 V per μs (or −1 volt over the 4 μs cycle hold time.)

The feedback of this "new" point position to U281 through R160 modifies the reference at pin 3 of Difference Amplifier U281 (new reference is one-half the output voltage at U282 pin 6). The next voltage from Input Buffer U170 is applied to the input (pin 2 of U281) of the Difference Amplifier which now amplifies the difference between the present point position on screen (represented by the voltage at pin 3 of U281A) and the new position (applied to pin 2 of U281A). This difference voltage is sampled and stored on Hold Capacitor C260 where it sets a new current level through R162 and R620 from the output of Voltage Follower U280 to the input (pin 2) of Integrator U282A.

This cycle just described of comparing the old position to the new one, sampling the difference, and ramping to the new position continues for each point of a vector waveform display.

The adjustment associated with Voltage Follower U280 is INT ADJ potentiometer R620. This pot (the integrator adjustment) is used to compensate for charge current introduced from analog switch U270B. A corresponding adjustment is not present in the Horizontal Vector Generator circuit. A VECTOR COMP adjustment is present in both the Vertical and Horizontal Integrator circuits. The pots (R276 vertical and R376 horizontal) are used to adjust for minimum vertical and horizontal offset between the vector and dot displays.

Mode Select

The Mode Select Switch consists of data selector U290A (horizontal) and U290B (vertical). The switches route the various X-Axis and Y-Axis signal sources to the Horizontal and Vertical Output Amplifiers. The select signals to U290 coming from Miscellaneous Display Register U540 (diagram 17) allow the System μP to switch to the various display modes (Envelope, vectors, dots, and readout). The System μP does this by writing control bits to the 1Q and 2Q output of Display Register U540 (AMP1 and AMP0 respectively) which are applied to select input SEL_B (pin 9) of U290B and to SEL_A (pin 10) of U290A.

An envelope waveform display is produced by selecting the X0 and Y0 inputs of U290 to be switched to the Output Amplifiers. The signal applied to the Horizontal Output Amplifier for YT displays is the incrementing count from the Display Counter, and it moves the electron beam horizontally across the face of the crt. In the Vertical circuitry, a sample-and-hold circuit formed by Data Selector U270A and Hold Capacitor C912 bypasses the Vertical Vector Generator circuitry. The 250 kHz signal driving the data selector, derived from the same Clock Divider circuit that supplies the $\overline{\text{SAMPLE}}$ signal (U410A and B, diagram 17), is delayed slightly by the rc combination of R607 and C900. The delay allows the analog signal at the output of the Vertical DAC to settle before the sample from Input Buffer Amplifier U170 is taken. The voltage on C912 is applied to the rc integrator made up of R165 and C166 to produce a min-max envelope with shaded vectors between the successive dots.

To produce a vector display of a waveform, the System μP selects the X1 and Y1 inputs of U290. This routes the outputs from the Vector Generators (previously described) to the Horizontal and Vertical Output Amplifiers.

For non-vector waveform displays, the X2 and Y2 inputs are routed to the outputs of U290. These signal lines, V DOTS and H DOTS, come directly from the output of the Vertical and Horizontal Input Buffers (U170 and U370B), bypassing the Vector Generators. Since the data applied to the Horizontal DAC in YT mode is from the incrementing Display Counter, the Y-Axis vertical deflections are displayed versus a linear X-Axis ramp (horizontal time axis). If XY mode is in effect, the data applied to the Horizontal DAC is the digitized waveform data used to provide the X-Axis deflection signal. In either YT mode with vectors off or XY mode, a dot waveform display is seen on the crt.

To display readout, the H READOUT and V READOUT signals at the Y3 and X3 inputs are switched to the outputs of U290. The resistive divider formed by R171 and R282 slightly decreases the amplitude of the signal from the Vertical DAC to ensure that all the Readout vertical data points are limited to eight vertical graticule divisions and will appear on screen. Operational amplifier U392B and its associated resistors perform the opposite function on the H READOUT signal from the Horizontal DAC, increasing the gain of that signal. This horizontal expansion causes the center 40 characters of a displayed readout line (out of a possible 64) to horizontally fill the screen. (See the Readout State Machine description for further details.)

Horizontal and Vertical Output Amplifiers

Operation and circuitry of the Horizontal and Vertical Output Amplifiers is nearly identical. Therefore, only the Horizontal Output Amplifier circuit operation is described.

The selected horizontal signal from U290A is applied to operational amplifier U392A configured with a variable gain set by R586. (The corresponding buffer in the Vertical Output Amplifier has a slightly different variable gain range.) Operational amplifier U392D is an inverting amplifier having a gain of about two. Horizontal offset is adjusted with R587.

The output of U392D drives the negative horizontal-deflection plate (H−) of the crt and operational amplifier U392C. Operational amplifier U392C is configured as an inverting buffer with unity gain, and its output drives the positive horizontal-deflection plate (H+).

Spot-Wobble Correction

The Spot-Wobble Correction circuit provides a dynamic correction of spot-shift on the crt caused by signal intensity changes (crt electron-beam current changes). Correction is accomplished by injecting offsetting currents that vary linearly with beam-current changes into the Vertical and Horizontal Output Amplifiers.

The beam-current control voltage is inverted by U460A and applied to one end of R583 and R584 while the other end of both potentiometers is connected to the noninverted control signal. Each potentiometer is adjusted over this "differential" range to minimize the associated spot wobble while viewing a special calibration display provided with the Extended Calibration function.

HIGH-VOLTAGE SUPPLY AND CRT

The High-Voltage Power Supply and CRT circuit (diagram 19) provides the voltage levels and control circuitry for operation of the cathode-ray tube (crt). The circuitry consists of the High-Voltage Oscillator, the High-Voltage Regulator, the +61 V Supply, the Cathode Supply, the Anode Multiplier, the DC Restorer, Focus and Z-Axis Amplifiers, the Auto Focus Buffer, the CRT, and the various CRT Control circuits.

High-Voltage Oscillator

The High-Voltage Oscillator transforms power obtained from the −15 V unregulated supply into the various ac levels necessary for the operation of the crt circuitry. The circuit consists primarily of transformer T525 and switching transistor Q628 connected in a power oscillator configuration. Sinusoidal low-voltage oscillations set up in the primary winding of T525 are raised by transformer action to high-voltage levels in the secondary windings. These ac secondary voltages are applied to the +61 V Supply, the DC Restorer, the Cathode Supply, and the Anode Multiplier circuits that provide the necessary crt operating potentials.

Oscillation occurs due to the positive feedback from the primary winding (pin 4 to pin 5) to the smaller base-drive winding (pin 3 to pin 6) used to provide base drive to switching transistor Q628. The frequency of oscillation is approximately 50 kHz and is determined primarily by the parallel resonance frequency of the transformer.

OSCILLATION START UP. Initially, when power is applied, the High-Voltage Regulator circuit detects that the crt cathode voltage is too positive and pulls pin 3 of

transformer T525 negative. The negative level is applied to the base of switching transistor Q628 through the transformer winding and forward biases it. Charge begins to flow in the primary winding through the transistor collector circuit and produces a magnetic field around the transformer primary winding. The increasing magnetic field induces an in-phase voltage in the base-drive winding that further supports the base-emitter voltage bias of the transistor. This in-phase feedback causes Q628 to remain on and continue supplying energy to the parallel resonant circuit formed by the winding inductance and interwinding capacitance of the transformer. As the primary voltage peaks, then begins falling, the induced magnetic field begins to decay. This decreases the base-drive voltage through the base-connected winding and begins to turn Q628 off.

As Q628 turns off, the magnetic field around the primary winding continues to collapse, and a voltage of opposite polarity is induced in the base-drive winding. This turns the switching transistor completely off. Once again, as the magnetic field builds and then reverses, the voltage induced in the base-drive winding changes direction, forward biasing Q628. At that point, the primary winding current starts increasing again, and the switching transistor is again turned on hard by the feedback supplied to the base-drive winding. This sequence of events occurs repetitively as the circuit continues to oscillate.

The oscillating magnetic field couples power from the primary winding into the secondary windings of the transformer. The amplitudes of the voltages induced in the secondary windings are a function of the turns ratios of the transformer windings.

High-Voltage Regulator

The High-Voltage Regulator consists of U168A and associated components. It monitors the crt Cathode Supply voltage and varies the bias point of the switching transistor in the High-Voltage Oscillator to hold the Cathode Supply voltage at the nominal level. Since the output voltages at the other secondary winding taps are related by turns ratios to the Cathode Supply voltage, all voltages are held in regulation.

When the Cathode Supply voltage is at the proper level (−1900 V), the current through R263 and the 19 MΩ resistor internal to High-Voltage Module CR565 holds the voltage developed across C260 at zero volts. This is the balanced condition and sets the output of integrator U168A at a level providing correct base drive for Q628 to hold the secondary voltages at their proper levels.

If the Cathode Supply voltage level tends too positive, a slightly positive voltage will develop across C260. This voltage causes the output of integrator U168A to move negative. The negative shift charges capacitor C717 to a different level around which the induced feedback voltage at the base-drive winding will swing. The added negative bias causes Q628 to turn on earlier in the oscillation cycle, delivering more energy per cycle to the resonant transformer. The increased energy in the resonant circuit increases the secondary voltages until the Cathode Supply voltage returns to the balanced condition (zero volts across C260). Opposite action occurs should the Cathode Supply voltage tend too negative.

+61 Volt Supply

The +61 Volt Supply circuit provides power to several other circuits on the High-Voltage board. Diode CR411 provides half-wave rectification of the first-tap voltage from the secondary of T525 and stores that charge on C317. Transistor Q215, zener diode VR210 and the associated components form a buffered zener regulator. Diode CR315 protects the base-emitter junction of Q215 should a failure reverse-bias the junction. Capacitor C218 stores a relatively large charge at the regulated level and supplies operating current to the load during current surges.

Cathode Supply

The Cathode Supply circuit is composed of a voltage-doubler and an rc filter network contained within High-Voltage Module CR565. This supply produces the −1900 V accelerating potential to the CRT cathode and the −900 V slot lens voltage. The −1900 V supply is monitored by the High-Voltage Regulator to maintain the regulation of all voltages from the High-Voltage Oscillator.

The alternating voltage from pin 10 of transformer T525 (950 V peak) is applied to a conventional voltage-doubler circuit at pin 7 of the High Voltage Module. On the positive half cycle, the input capacitor of the voltage doubler (0.006 μF) is charged to −950 V through the forward-biased diode connected to ground at pin 9 of the module. The following negative half cycle adds its ac component (−950 V peak) to this stored dc value and produces a total peak voltage of −1900 V across the capacitor. This charges the 0.006 μF storage capacitor (connected across the two doubler diodes) through the second diode (now the forward-biased diode) to −1900 V. Two rc filters follow the voltage doubler to smooth out the ac ripple. A resistive voltage divider across the output of the filter network provides the −900 V slot lens potential.

Anode Multiplier

The Anode Multiplier circuit (also contained in High-Voltage Module CR565) uses voltage multiplication to produce the +14 kV CRT anode potential. Circuit operation is similar to that of the voltage-doubler circuit of the Cathode Supply.

The first negative half cycle charges the 0.001 μF input capacitor (connected to pin 8 of the High Voltage Module) to a positive peak value of +2.33 kV. The following positive half cycle adds its positive peak amplitude to the voltage stored on the input capacitor and boosts the charge on the second capacitor of the multiplier (and those following) to +4.66 kV. Following cycles continue to boost up succeeding capacitors to values +2.33 kV higher than the preceding capacitor until all six capacitors are fully charged. This places the output of the last capacitor in the multiplier at +14 kV above ground potential. Once the multiplier reaches operating potential, succeeding cycles replenish charge drawn from the Anode Multiplier by the crt beam. The 1 MΩ resistor in series with the output protects the multiplier by limiting the anode current to a safe value.

Focus Amplifier

The Focus Amplifier, in conjunction with the auto-focus circuitry, provides optimum focus of the crt beam for all settings of the front-panel INTENSITY control. The Focus Amplifier itself consists of two shunt-feedback amplifiers composed of Q145, Q152, and their associated components. The outputs of these amplifiers set the operating points of a horizontally converging quadrapole lens and a vertically converging quadrapole lens within the crt. The convergence strength of each lens is dependent on the electric field set up between the lens elements.

Since the bases of Q145 and Q152 are held at constant voltages set by their emitter potentials, changing the position of the wiper arms of the ASTIG and FOCUS pots changes the current in the base resistors, R261 and R145. This changes the feedback currents in R245 and R246 and produces different output levels from the Focus Amplifiers; that in turn, changes the convergence characteristic of the quadrapole lenses.

Initially, at the time of adjustment, the FOCUS and ASTIG potentiometers are set for optimum focus of the crt beam at low intensity. After that initial adjustment, the ASTIG pot normally remains as set, and the FOCUS control is positioned by the user as required when viewing the displays. When using the FOCUS control, transistor Q152 is controlled as described above; however, an additional current is also supplied to the base node of Q145 from the FOCUS pot through R262. This additional current varies the base-drive current to Q145 and provides tracking between the two lenses as the FOCUS control is adjusted during use of the instrument.

Auto Focus Buffer

The convergence strengths of the quadrapole lenses also dynamically track changes in the display intensity. The VQ signal, applied to the crt at pins 5 and 6, is linearly related to the VZ (intensity) signal driving the crt control grid, and increases the strength of the lenses at higher crt beam currents. (A higher beam current requires a stronger lens to cause an equal convergence of the beam.) The emitter follower Q500 buffers the VZ signal (offset 15 volts by VR316) to the first and second quadrapole lenses. A linear relationship (as opposed to the "ideal" exponential relationship) between the Z-Axis drive (VZ) and quadrapole voltage (VQ) provides adequate dynamic focusing for low to medium Z-Axis drive. The High-Drive Focus adjustment R400 sets the attenuation factor at the output of buffer Q500. Capacitors C409 and C295 compensate for the capacitive loading of the quadrapole elements.

Z-Axis Amplifier

The high-voltage, high-speed transresistance amplifier U227 produces VZ, the Z-Axis drive signal. The amplifier has two signal inputs: ZINT—a current input that determines the output voltage VZ, and $\overline{\text{ZON}}$—a TTL gating signal that causes VZ to go to its lowest value (approximately 8 V) when HI. Capacitor C139 supplies current to U227 during VZ transitions, R137 is a current limiter, and C234 is a bootstrap capacitor to speed up VZ edges.

DC Restorer

The DC Restorer provides crt control-grid bias and couples both the dc and the low-frequency components of the Z-Axis drive signal to the crt control grid. This circuit allows the Z-Axis Amplifier to control the display intensity by coupling the low-voltage Z-Axis drive signal (VZ) to the elevated crt control grid potential (about −1.9 kV). Refer to Figure 3-10 for the following description.

The DC Restorer circuit operates by clipping an ac voltage waveform at the grid bias and the Z-Axis drive levels. The shaped ac waveform is then coupled to the crt control grid through a coupling capacitor that restores the dc components of the signal.

GRID BIAS LEVEL. An ac drive voltage of approximately 300 V peak-to-peak is applied to the DC Restorer circuit from pin 7 of transformer T525. The negative half-cycle of the sinusoidal waveform is clipped by CR541, and

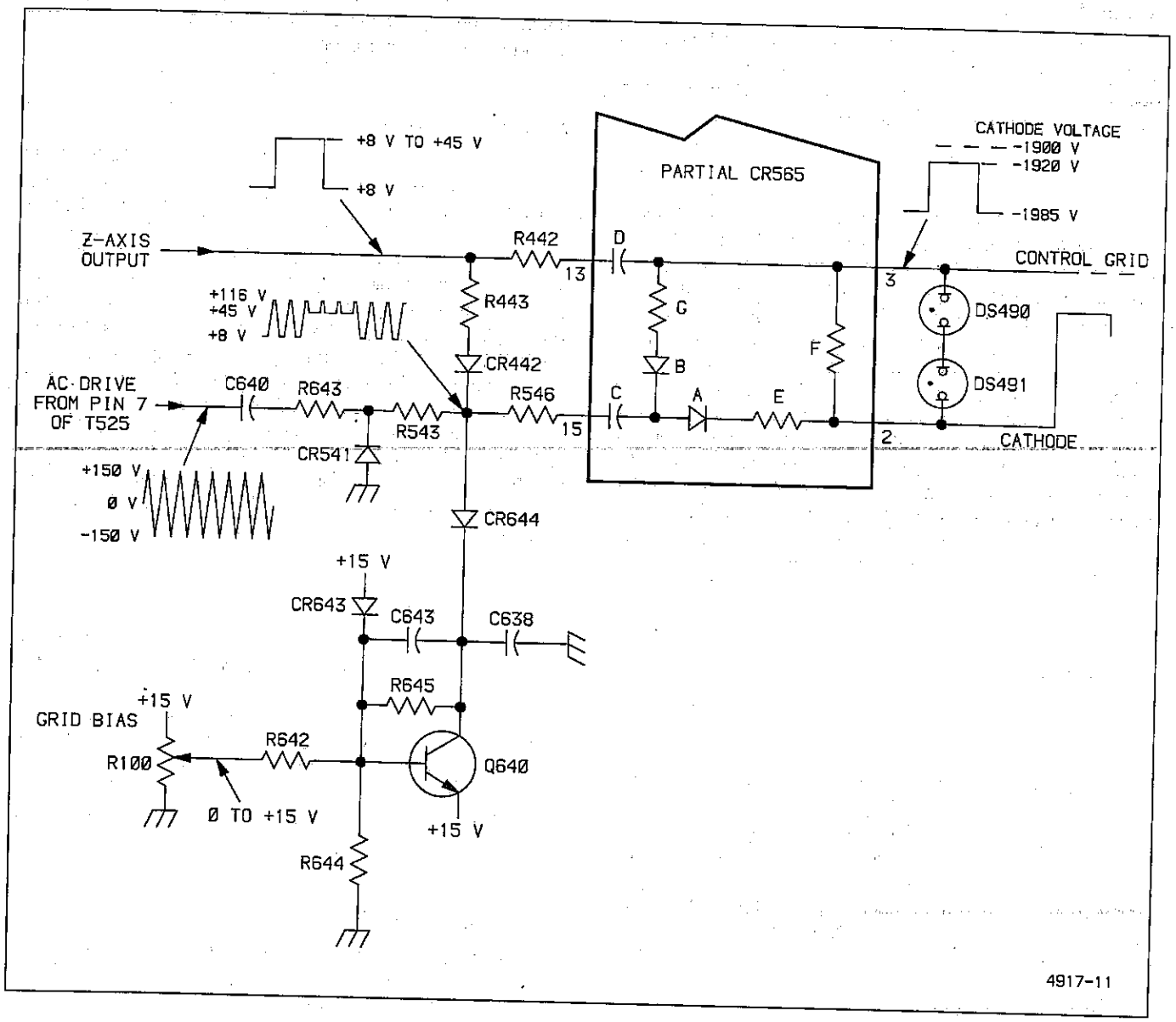


Figure 3-10. DC Restorer.

the positive half-cycle (150 V peak) is applied to the junction of CR442, CR644, and R546 via R643 and R543. Transistor Q640 and associated components form a voltage clamp circuit that limits the positive swing of the ac waveform at the junction.

Transistor Q640 is configured as a shunt-feedback amplifier with C643 and R645 as the feedback elements. The feedback current through R645 develops a voltage across the resistor that is positive with respect to the +15.6 V on the base of the transistor. The value of this additive voltage plus the diode drop across CR644 sets the clamping threshold. Grid Bias potentiometer R100 varies the voltage across base resistor divider R642 and R644 and thus sets the feedback current through R645. The adjustment range of the pot can set the nominal clamping level between +45 V and +75 V.

When the amplitude of the ac waveform is below the clamping threshold, diode CR644 will be reverse biased and the ac waveform is not clamped. During the time the diode is reverse biased, transistor Q640 is kept biased in the active region by the charge retained on C643 from the previous cycle. As the amplitude of the ac waveform at the junction of CR442 and CR644 exceeds the voltage at the collector of Q640, diode CR644 becomes forward biased, and the ac waveform is clamped at that level. Any current greater than that required to maintain the clamp voltage will be shunted to the +15 V supply by transistor Q640.

Z-AXIS DRIVE LEVEL. The variable Z-Axis signal (VZ) establishes the lower clamping level of the ac waveform applied to the High Voltage Module. When the amplitude of the waveform drops below the Z-Axis signal level, CR442 becomes forward biased, and the ac waveform is clamped to the Z-Axis signal level. The VZ level may vary between +8 V and +50 V, depending on the setting of the front-panel INTENSITY control.

The ac waveform, now carrying both the grid-bias information and the Z-Axis drive information, is applied to a DC Restorer circuit in the in the High-Voltage Module where it is lowered to the voltage level of the crt control grid (approximately −2 kV).

DC RESTORATION. The DC Restorer circuit in the High-Voltage Module is referenced to the crt cathode voltage via a connection within CR565. Capacitor C (labeling shown in Figure 3-10), connected to pin 15 of CR565, initially charges to a level determined by the difference between the Z-Axis signal level and the crt cathode potential. The Z-Axis signal sets the level on the positive plate of capacitor C through R443, CR442, and R546; the level on the negative plate is set by the crt cathode voltage through resistor E and diode A. Capacitor D is charged to a similar dc level through resistor F and R442.

When the ac waveform applied to pin 15 begins its transition from the lower clamped level (set by the Z-Axis signal) towards the upper clamped level (set by the Grid Bias potentiometer), the charge on capacitor C increases. The additional charge is proportional to the voltage difference between the two clamped voltage levels.

When the ac waveform begins its transition from the upper clamped level back to the lower clamped level, diode A becomes reverse biased. Diode B becomes forward biased, and an additional charge proportional to the negative excursion of the ac waveform (difference between the upper clamped level and the lower clamped level) is added to capacitor D through diode B and resistor G. The amount of charge added to capacitor D depends on the setting of the front-panel INTENSITY control, as it sets the lower clamping level of the ac waveform. This added charge determines the potential of the control grid with respect to the crt cathode.

The potential difference between the control grid and the cathode controls electron-beam current (the display intensity). With no Z-Axis signal applied (INTENSITY control off), capacitor D will be charged to its maximum negative value since the difference between the two clamped voltage levels is at its maximum value. This is the minimum intensity condition and reflects the setting of the Grid Bias potentiometer. During calibration, the Grid Bias pot is adjusted so that the difference between the upper clamping level (set by the Grid Bias pot) and the "no signal" level of the Z-Axis drive signal (VZ) produces a control grid bias that barely shuts off the crt electron beam.

As the INTENSITY control is advanced, the amplitude of the square-wave Z-Axis signal increases accordingly. This increased signal amplitude decreases the difference between the upper and lower clamped levels of the ac waveform, and less charge is added to capacitor D. The decreased voltage across capacitor D decreases the potential difference between the control grid and the cathode, and more crt beam current is present. Increased beam current increases the crt display intensity.

During the periods that capacitor C is charging and discharging, the control grid voltage is held stable by the long-time-constant discharge path of capacitor D through resistor F. Any charge removed from capacitor D during the positive transitions of the ac waveform will be replaced on the negative transitions.

The fast-rise and fast-fall transitions of the Z-Axis signal are coupled to the crt control grid through capacitor D. This ac-coupled fast-path signal sends the crt electron beam to the new intensity level, then the slower DC Restorer path "catches up" to handle the dc and low-frequency components of the Z-Axis drive signal.

Neon lamps DS490 and DS491 prevent arcing inside the crt by preventing the control grid and cathode from becoming too widely separated in voltage.

Other CRT Control Circuits

The CRT Control Circuits produce the voltages and current levels necessary for the crt to operate. Operational amplifier U168B, transistor Q269, and associated components form an Edge-Focus circuit that establishes the voltages for the elements of the third quadrapole lens. The positive lens element is set to its operating potential by Edge Focus adjustment pot R300 (via R393). This voltage is also divided by R278 and R277 and applied to the noninverting input of U168B to control the voltage on the other element of the third lens.

The operational amplifier and transistor of the Edge-Focus circuit are arranged as a feedback amplifier with R279 and R179 setting the stage gain. Gain of the amplifier is equal to the attenuation factor of divider network R278 and R277; so, total overall gain of the stage from the wiper of R300 to the collector of Q269 is equal to unity. The offset voltage between lens elements is set by the ratio of R279 and R179 and the +10 V reference applied to R179. This arrangement causes the two voltages applied to the third quadrapole lens to track each other over the entire range of Edge Focus adjustment R300.

Other adjustable level-setting circuits include "Orthogonality" Alignment pot R305, used to rotate the beam alignment after vertical deflection. This adjustment controls the amount of current through the Y-Axis alignment coil around the neck of the crt and is set to produce precise perpendicular alignment between the X- and Y-Axis deflections. The TRACE ROTATION adjustment pot, R1077, is a front-panel control. The effect of the adjustment is similar to the Y-Axis Alignment pot, but when adjusted, it rotates both the X-Axis and the Y-Axis deflections on the face of the crt. A final adjustable level-setting control is the Geometry pot R200, adjusted to optimize display geometry.

SYSTEM I/O

The System I/O circuits (diagram 20) provide methods of getting various types of signals or voltages into and out of the scope. These include a GPIB interface, an interface to the AutoStep Sequencer, Word-Trigger interface, an audio bell, and the probe-power connectors used to supply power to active probes.

GPIB

The GPIB interface provides an electrical interface adherent to the IEEE 488-1980 Standard using protocols defined in the Tektronix GPIB Codes and Formats Standard.

GPIB data transfers are done under control of U630, a GPIB Controller integrated circuit. The controller automatically produces proper handshaking and data direction control. Data is transferred to and from the GPIB bus through bidirectional buffer U624. Handshaking signals are transferred to and from the GPIB bus via the handshaking bidirectional buffer, U720. Data transfers between the GPIB Controller and the System μP are through bidirectional buffer U532.

When power is first applied, the $\overline{\text{GPIBRESET}}$ signal from register U754 holds GPIB Controller U630 in its reset state. The System μP then removes the reset and begins to initialize the internal registers of the GPIB Controller. To write data into the registers, the System μP writes data to the memory-mapped addresses between 6800h and 6807h. These addresses produce a LO $\overline{\text{GPIBSEL}}$ and a LO address bit A3 applied to U332B and enable the GPIB Controller. Data is written to the internal register defined by address bits A0-A2.

The GPIB Controller is now initialized and begins watching the handshake lines on the GPIB bus, looking for a data transfer to be initiated by another GPIB device on the bus. Data transfer may also be initiated by the System μP by writing data into the GPIB Controller data register. In either case, activity on the GPIB bus follows the sequences presented in Figures 3-11 and 3-12.

When data has been read into the controller from the GPIB bus, the $\overline{\text{GPIBINT}}$ (GPIB Interrupt) request is asserted, telling the System μP that GPIB data is available. To receive the data, the System μP reads the GPIB Controller internal data register, automatically resetting the interrupt request.

Status of the GPIB operations is displayed on the three front-panel GPIB Status LEDs. These LEDs are turned on or off by the System μP by writing three control bits into Word Probe and GPIB LED Register U754.

See the Programmers Reference Guide included with this instrument for the GPIB commands and functions implemented in this scope.

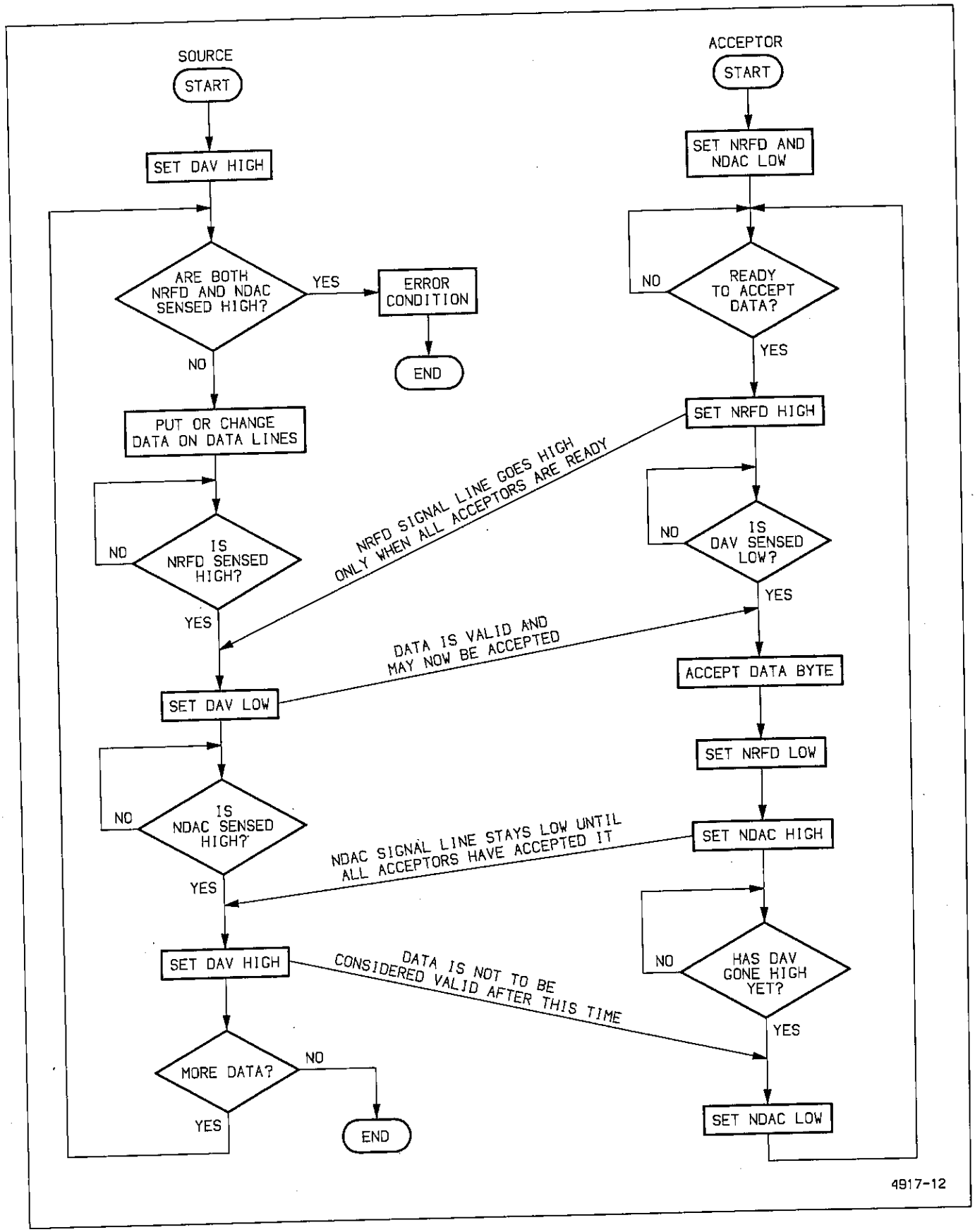


Figure 3-11. GPIB data flow diagram.

The GPIB may be set up to operate with a Think-Jet® printer or any plotter using the Hewlett-Packard Graphic Language® as a listen-only device on the bus. No controller may be used, and the printer/plotter should be the only device other than the 2440 on the bus.

Sequencer Output Circuit

The Sequencer Output circuit drives two output BNC connectors and accepts input from a third BNC connector. The outputs/input are called SEQUENCE OUT, STEP COMPLETE, and SEQUENCE IN, respectively. SEQUENCE OUT steps LO (TTL level) to indicate when a sequence completes execution; STEP COMPLETE steps LO to indicate when a step in a sequence completes. A TTL step from HI to LO (or grounding the input) to SEQUENCE IN restarts a temporarily halted sequence. See the Operators Manual included with this instrument for more information.

The System μP controls the SEQUENCE OUT and STEP COMPLETE output levels via Miscellaneous Register U760 (diagram 1). When a sequence and/or step is complete, the System μP sets SEQOUT and/or STEP COMP HI out of the Miscellaneous Register.

SEQOUT is coupled to Q104 via R300, a 1kΩ resistor. A TTL HI voltage level, dropped across the R330 and the base/emitter of Q104, is great enough to saturate Q104 and provides a LO SEQUENCE OUT at J1903. When SEQOUT is LO, Q104 is off. SEQUENCE OUT at J1903 is pulled up to about +3V via R108. (The +5 Volt supply is zener-regulated by R105 and VR 105 to provide the +3 Volt collector supplies for Q104 and Q107.)

The circuit action of Q107 and its surrounding circuitry is identical to the Q104 stage with STEP COMP driving the base of Q107 via R108 to provide STEP COMPLETE at J1904. CR104/CR107 provide output protection for Q104/Q107.

To read the SEQUENCE IN at J1905, the System μP periodically sets $\overline{\text{SEQINCS}}$ (Sequence In Chip Select) LO via Miscellaneous Register U884 (diagram 1). SEQINCS is routed to one input of OR-gates U250C and U132A; the other input of OR-gate U250C is connected to the System μP $\overline{\text{WR}}$ (write) line, and the other input of U132A is connected to the System μP $\overline{\text{RD}}$ line. With SEQINCS LO, the $\overline{\text{WR}}$ and/or $\overline{\text{RD}}$ can drive the output of their respective OR-gate LO, when they are asserted.

After setting SEQINCS LO, the System μp next asserts $\overline{\text{WR}}$ LO. This LO drives the output of OR-gate U250C LO to RESET the Q output of D-type Flip-Flop U894B LO. NEXT, $\overline{\text{RD}}$ is asserted LO ($\overline{\text{WR}}$ goes HI) to drive the out-

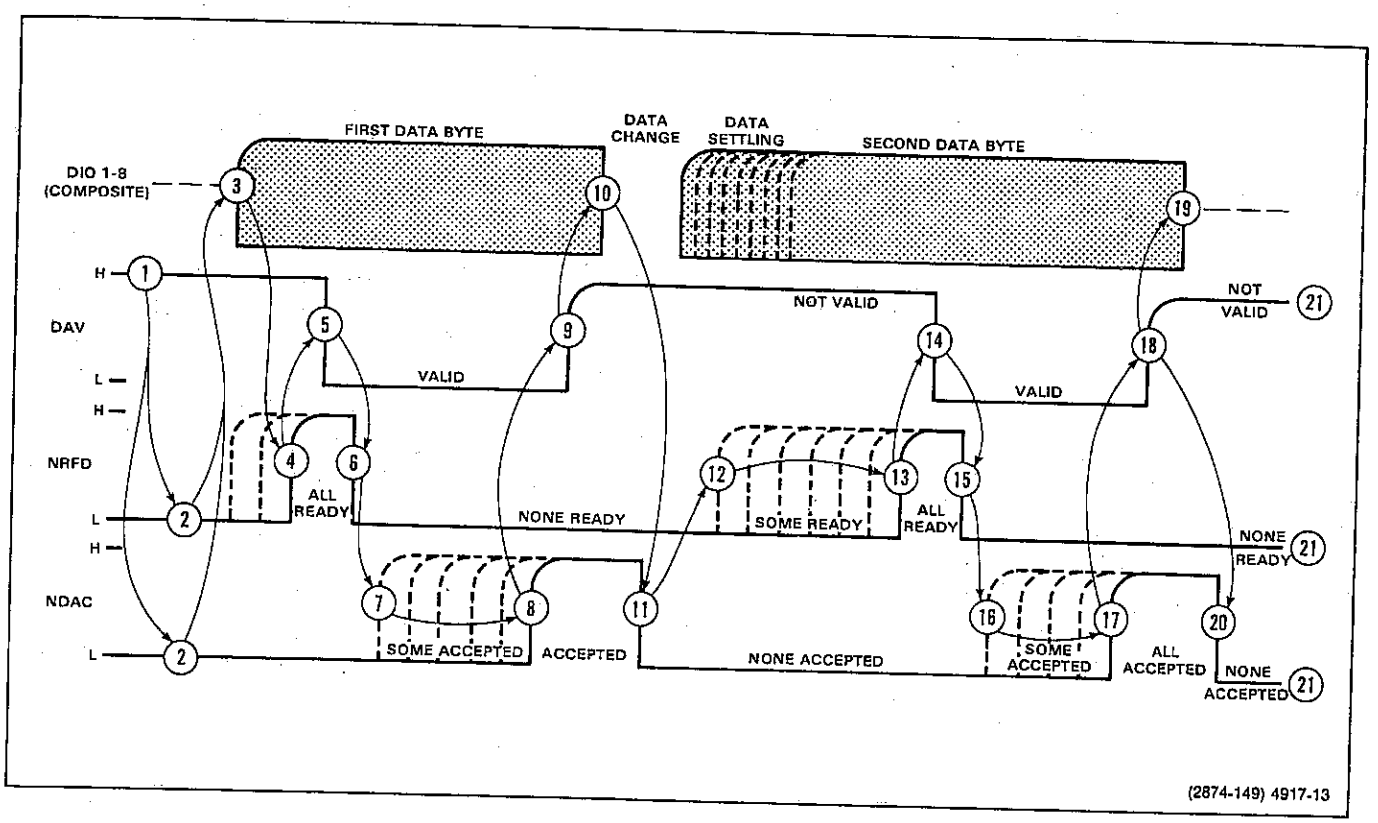


Figure 3-12. GPIB three-wire handshake state diagram.

put of OR-gate U132A LO. This LO enables the upper-four buffers of the Octal Buffer U120. With the Q-output of Flip-Flop U894B connected to the input of one of the enabled buffers, that reset-forced LO obtained at $\overline{WR}$ is coupled to the D0 line of the System μP Data Bus. The System μP monitors the D0 bit as long as $\overline{RD}$ and SEQINCS are asserted.

The input to inverter U424E is normally pulled up to +5 volts by R120. This HI is inverted LO by U424E and routed to the positive-triggered clock input of Flip-Flop U894B. If, during the time $\overline{RD}$ is asserted, SEQUENCE IN steps LO at J1905, it drives the clock input of U894B HI and the +5 volts hardwired to the D-input of the flip-flop latches to the Q output. With the Quad Buffer still enabled by $\overline{RD}$, the System μP reads the transition via data bit D0 and restarts the temporarily-halted sequence.

Word Trigger and GPIB Status Control Register

The Word Trigger circuit provides interface and control of the external Word Trigger Probe. Two bits from Control Register U754 are used to set the recognition mode of the Word Trigger Probe. Forty bits of serial data are applied to the W DATA (word data) line and clocked into the serial shift register in the word probe by toggling the W CLOCK (word clock) line. Once loaded, the Word Trigger Probe outputs a trigger pulse each time (and as long as) the set conditions are met.

The $\overline{WDTTL}$ output is applied to the trigger circuits where, if selected as the trigger source, it produces a scope trigger event. The trigger signal is buffered to the rear panel by U844D, Q720, and the associated components. Output levels are TTL compatible, with the maximum HI level being set by R716 and VR717. Output impedances are 47 ohms LO and 227 ohms HI. Diode CR722, zener VR717, and resistors R717 and R718 provide protection of the output circuit should an out-of-range voltage be applied to the output connector.

The remaining inputs and outputs of Control Register U754 are used to control the GPIB Status LEDs and to reset GPIB Controlier U630.

Bell

The Bell circuit allows the scope to produce an audio tone to draw the operator's attention to certain warning and error conditions. The circuit consists of a free-running oscillator whose signal is gated through the output speaker.

The oscillator consists of timer U274, configured as an astable multivibrator (oscillator), and output transistor Q594, used to buffer the oscillator output. Current flowing in R274 and R276 charges C372 up until it crosses the trigger level at pin 2 of U274. This sets the output applied to the base of Q594 LO, turning the transistor off, and sets the discharge output at pin 7 to ground potential. Capacitor C372 now discharges through R276 until the threshold level at pin 6 is reached, at which time the output at pin 3 goes HI and the discharge pin goes to a high-impedance state. Capacitor C372 begins to charge through R274 and R276 again, completing the cycle. The cycle continues as long as instrument power is applied, alternately turning Q594 off and on with an approximate 50% duty cycle.

The BELL line from the Miscellaneous Register (U760, diagram 1) is used to gate this oscillator signal through the speaker to produce the audio output. As long as BELL is LO, transistors Q596, Q558, and Q592 are off, and current is cut off to speaker LS498.

When BELL goes HI, transistor Q596 turns on, which in turn, turns on Q588. With Q588 on, the base of Darlington transistor Q592 is pulled HI. Now, whenever the oscillator transistor Q594 is on, proper biasing conditions for Q592 are established and current flows from the +5 V_D supply to ground through Darlington Q592, the speaker LS498, and transistor Q594. When Q594 turns off, current flow is interrupted until the oscillator turns Q594 back on.

Since LS498 is inductive, the current decay portion of its cycle (Q594 off) tends to force pin 1 of the speaker above the +5 V_D supply level. Diode CR594 becomes forward biased in this case and shunts the decay current back to the +5 V_D supply, protecting transistor Q594 from overvoltage conditions.

As long as the BELL line remains HI, the speaker produces an approximate 2 kHz tone. In practice, the System μP sets the BELL line HI for a short time ($\simeq$4 ms), turning Q588 on, starting the tone and rapidly charging C590. When BELL returns LO, C590 gradually discharges through R594. As the capacitor discharges, bias on Q592, and thus current through the speaker, is reduced, causing the sound to gradually fade out in a pleasing "bell-like" tone.

Probe Power

The Probe Power outputs on the rear panel provide access to three of the instrument power-supply voltages and may be used to power approved voltage- and current-probe accessories. Contact your Tektronix sales representative for a list of approved probe accessories.

Video Option Control Register

The Video Option Control Register (U750 on diagram 20) is written to by the System Processor (address-decoded location 6012h) to control operational setup of the Video Option. The Video Option Control Register is initialized on power-up and provides for control of the following functions:

1. Selection of trigger field (Field1 or Field2).

2. Choice of triggering on positive- or negative-sync input signals (NEG-SYNC).

3. Selection of correct polarity of the offset signal via the CH2 INV signal.

4. Control of the display functions (VIDEO CLAMP and FAST CLAMP).

5. Enabling the Video Trigger Circuit to trigger the scope.

6. Selection of TV Line Coupling—allowing all lines to produce a trigger signal to the main Trigger circuit of the scope.

VIDEO OPTION

The Video Option (diagram 21) consists of additional hardware and firmware installed in the host instrument to enhance triggering on and viewing of composite video signals. The Video Option block diagram located in the tabbed foldout pages in the rear of the manual may be an aid in following the Video Option circuit descriptions.

The Video Option circuitry contains both video-signal processing and trigger-generation circuits. The video-signal processing circuits stabilize the input signal and separate the television synchronization signals (horizontal and vertical sync pulses) from the composite video signal. The trigger-generation circuits then count these separated sync pulses to determine when a TV Trigger signal is to be produced.

In the video-signal processing circuits, the gain of the AGC (automatic gain control) Amplifier is automatically adjusted to produce the correct signal amplitude to the Sync Pickoff Comparator for proper sync separation over a wide range of input signal levels. The Trigger Back-Porch Clamp adjusts the back-porch level of the input signal through the Fixed-Gain Amplifier on each sync pulse. The feedback to the Fixed Gain Amplifier compensates for level shifting caused by any power-line ripple riding on the composite video signal. The Sync-Tip Clamp circuit monitors the horizontal-sync pulse amplitude and produces the automatic-gain-control voltage that sets the gain of the AGC Amplifier. Sync pulses are separated from the composite video signal by the Sync Pickoff Comparator. The horizontal- and vertical-sync pulses are further separated by the Pulse Stretcher and Field Generator circuits for use in producing the horizontal clock and field-sync signals needed by the Trigger Generation circuitry.

To set up the Video Option operating modes, the System Processor writes control settings to the Video Mode Option Register (diagram 20) in the System I/O circuitry. The latched setting in the register is held until a different mode is needed. Programmable counters, also under System processor control, count the extracted horizontal sync pulses (lines) until the line number for the selected trigger point is reached. At that point, if the main trigger circuit is finished with holdoff, the TV Trigger Generator circuit produces a TV Trigger to the A/B Trigger Generator to trigger the next storage acquisition.

An additional display function added to Channel 2 is the TV CLAMP feature. When enabled, the circuitry holds the back-porch level of the displayed signal on Channel 2 at ground level. The Channel 2 Vertical Display Clamp circuit checks the back-porch levels of the incoming TV signal on Channel 2 and produces offsetting voltages to the Channel 2 Preamplifier to bring those levels back to ground reference. The circuit action produces a stable vertical signal display of a TV signal by removing power supply ripple that may be present. Either inverted or noninverted signals may be displayed with the TV CLAMP feature.

Video Signal Processing Circuitry

AGC AMPLIFIER. The AGC (automatic gain control) Amplifier, Q514, U612, and U710B, amplifies the composite-video input signal from the selected trigger channel. Stage gain is controlled by feedback that is derived from the amplitude of the incoming horizontal sync pulses. The amplifier itself is formed by two cross-connected differential amplifier pairs in U612 that permit normal or inverted amplification of the signal. The front-panel SLOPE/SYNC switch selects whether the amplifier is inverting or noninverting to match the required signal polarity for the sync-separation circuits. For correct operation of the sync separation circuit, the composite-video signal must be sync-negative; therefore, if a "noninverted" signal display has positive sync, the SLOPE/SYNC switch may be pressed to invert the signal (+ SLOPE LED is on for positive-sync input display). Inversion only occurs in the trigger Sync Separator path; the display polarity remains unaffected.

Gain of the AGC Amplifier is controlled by the action of the Trigger Back-Porch Clamp, the Sync-Tip Clamp, and the Automatic Gain-Control circuitry working together to set the channel resistance of FET Q514 and thereby the gain of AGC Amplifier U612. Amplifier gain is automatically adjusted to maintain the sync-tip level at a known point relative to the back-porch amplitude of the signal. This action provides an accurate and stable pickoff point on the signal to the Sync Pickoff Comparator circuit (Q504 and Q510) with input video signals of different or varying amplitudes. The minimum gain of the circuit is decreased (to permits the application of higher amplitude signals) by the use of constant-current diodes CR526 and CR620 as the current sources for the differential amplifiers.

When power is first applied, the operating level of the AGC Amplifier is established by feedback only. With no

signal applied, the channel resistance of Q514 is minimum, setting the gain of the AGC Amplifier to maximum. With maximum gain and no signal, the feedback loops of the Back-Porch Clamp and the Sync-Tip Clamp set the circuit gain as if an average "ground" signal were being received.

The composite-video input signal is applied to one input of the differential AGC Amplifier at pin 3 of U612 and to Dc-Offset Amplifier U710B via a low-pass filter composed of R714 and C714. The low-pass filter averages the signal at the input of U710B so that only the average (dc) signal level appears at the output of U710B and on pin 11 of U612. Since the input signal swings about this average level, the AGC Amplifier output signal will be centered in its linear amplification region.

The base-emitter bias of the differential output transistors within U612 are controlled by the NEG-SYNC signal from Video Option Control Register U750 (diagram 20). When the NEG-SYNC bin is set HI, the transistors connected to pins 2 and 9 will be biased on, with those at pins 6 and 13 biased off. When NEG-SYNC is set LO, the conducting transistors are switched, and the polarity of the output signal driving transistor Q612 is inverted. Common-base transistor Q612 level shifts the output signal from the AGC Amplifier and provides voltage gain to drive U610D.

FIXED GAIN AMPLIFIER. The Fixed Gain Amplifier circuit, formed by U610A, B, and C, Q502, and U710C, provides additional gain to the video signal from the AGC Amplifier. The Trigger Back-Porch Clamp circuit monitors the back-porch level of the resulting signal and injects an offsetting dc level into the Fixed Gain Amplifier via U710C to shift that level to approximately +4.5 V.

Emitter-follower U610D drives one input of a differential amplifier made up of U610A and U610B, while the other input is driven by the output signal of U710C. Transistor U610C and its associated components form the current source for the amplifier. The collector output of U610B drives the input of the Sync Pickoff Comparator.

Transistor Q502 and its associated circuitry act as a start-up circuit that monitors the dc output level of U610B and applies an offset voltage to pin 10 of U710C should that level go below zero volts. This occurs when going from a "no-signal" or low-signal condition to a strong signal. If the dc output level goes below ground, diode CR612 will become forward biased, shutting off Q502. With Q502 off, the −15 V supply applied via resistor R506 will forward bias CR606 to charge C713 negatively. This pulls the output voltage of U710C negative and decreases base drive to U610B. Reducing base drive reduces the collector current so that the collector voltage of U610B returns positive until the above zero-volt output level is restored and CR612 becomes biased off.

SYNC PICKOFF COMPARATOR. The Sync-Pickoff Comparator, composed of Q504 and Q510, switches when the amplitude of a sync pulse crosses the comparator threshold level. The switching threshold is set by the biasing resistors of Q510, R408 and R409, to about 50% of the sync level to eliminate any video information. The output signal from the collector of Q510 is the composite of all detected sync pulses, and the output of Q504 is an inverted replica of that signal.

SYNC-TIP CLAMP AND AUTOMATIC GAIN CONTROL. Transconductance Amplifier U510, in conjunction with the AGC Amplifier, is used to clamp the sync-tip level. Amplifier U510 is enabled by the bias current supplied by Q512 when sync tips turn that transistor on. This amplifier acts as a weak operational amplifier to set the sync-tip level constant when Q512 is conducting to supply bias current to pin 5 of U510.

The Sync-Tip Clamp holds the negative-sync tips at about +0.5 V, so the resulting sync pulses are approximately 4 V in amplitude. Anytime the negative-sync tips at the collector of U610B go below about +0.5 V, input pin 3 of U510 will go below the ground reference at the other input. This causes the output of U510 to go low when enabled, and C512 begins discharging slowly toward −15 V. This decreasing voltage is applied to the gate of FET Q514 to increase the channel resistance and decrease the gain of the AGC Amplifier. Since U510 is a transconductance amplifier, it can change the voltage across C514 only a small amount during each sync pulse, and a few horizontal-line cycles are needed to reduce the gain of the AGC Amplifier to the new operating level. Between sync tips, when amplifier U510 is disabled, the long time constant of R610 and C512 holds the bias for Q514 (and thus gain of the AGC Amplifier) nearly constant.

Diode CR502 acts to reduce AGC Amplifier gain quickly if the negative-sync-tip amplitude at the collector of U610B drops below −0.8 V. If the diode becomes forward biased, as it might should the signal amplitude go suddenly negative, Q510 will be turned on for a longer time until the signal amplitude returns to a lower level. Amplifier U510 can then increase the channel resistance of Q514 more quickly to reduce gain of the AGC Amplifier and return the sync-tip amplitude to the correct level.

TRIGGER BACK-PORCH CLAMP. The Trigger Back-Porch Clamp circuit formed by U504, U410A, and associated components, is enabled for a short time during each horizontal-sync pulse immediately following the sync tip (during the back-porch time). The output of the Trigger Back-Porch Clamp is used to hold the back-porch level of the composite-video signal to a predetermined dc level. This, in combination with the action of the Sync-Tip Clamp, produces sync pulses that are approximately 4 V in amplitude.

Transconductance Amplifier U504 is enabled by turning transistor U410A off on the falling (trailing) edge of the inverted sync pulse from Q504 (via C308). Bias current to turn on U504 is then supplied through R403. The amplifier will stay enabled until the current supplied by resistor R214 charges C308 back positive enough to bias U410A back on (in approximately 1 μs). During the time that U504 is enabled, it senses the back-porch level of the composite-video waveform applied to pin 3 via resistive divider R613, R602, and R604. Depending on whether the sensed level is above or below the ground reference level on pin 2, the amplifier output will either charge or discharge capacitor C713 to a new voltage level. This will slightly change the offset voltage applied to pin 4 of U610B (via U710C), shifting the entire composite-video waveform in the direction required to hold the back-porch level at +4.5 volts (zero volts on pin 3 of U504). During the period between back porches, C713 acts as a hold capacitor to maintain the offset bias on U610B.

PULSE STRETCHER. The Pulse Stretcher lengthens the horizontal-sync pulse width to produce a more symmetrical, faster rise-time clocking pulse. It also removes alternate equalizing and serrated pulses that occur during the NTSC TV signal vertical-sync block from the composite-sync waveform in order to maintain the correct horizontal clock rate.

Transistors U420B, U420C, and associated components form a monostable multivibrator used to stretch the width of the horizontal-sync pulses. The leading edge of each horizontal-sync pulse turns on U420C which, in turn, reverse biases diode CR224 via C325 to turn off U420B. The resulting HI at the collector of U420B keeps U420C biased on (via R421). The output at the collector of U420B remains HI until C325 charges to about +1 volt via R224; then, CR224 becomes forward biased to once again turn U420B on. The collector voltage of transistor U420B then drops to about +0.4 V, at which point diode CR329 conducts to clamp the output at one diode drop above ground. This stretched output pulse from the monostable multivibrator is level-shifted down one diode drop through CR328 to produce the TTL-compatible HORIZCLK signal used to generate trigger signals to the main Trigger circuit of the oscilloscope.

Since the equalizing and serration pulses in the vertical-sync block occur at twice the horizontal-sync rate (see Figures 3-13 and 3-14), every other one must be prevented from triggering the monostable multivibrator to keep the line count correct. The DLY'D HCLK (delayed Horizontal clock) applied to the base of U420B (via R210) holds that transistor on for a period of time between the normal horizontal line-sync pulses. This action effectively removes the unwanted pulses from the HORIZCLK output by preventing them from triggering the multivibrator circuit.

CLOCK FREE RUN. If non-NTSC standard television signals are being used, the vertical-sync block may not be serrated. To maintain the proper horizontal-sync rate during the absence of signal-supplied horizontal pulses, the Clock Free-Run circuit produces "artificial" clock pulses. Therefore, the line count will continue and be correct when the next horizontal-sync pulse does arrive. The signal used as the self-generated HORIZCLK signal is derived from the VCO (voltage-controlled oscillator) output (2XH) of the Phase-Locked Loop circuit. That signal, at twice the horizontal-sync rate, is divided by two at the Q output of flip-flop U220B. It is then wire-ORed into the HORIZCLK signal line via R334 and CR332. If a horizontal-sync pulse is not present to trigger the monostable multivibrator, CR332 will be biased on by the HI HCLK to pass that pulse to the HORIZCLK signal line. When the Phase-Locked Loop (PLL) circuit is locked (synchronized) with the incoming horizontal sync, the HCLK rising edge will slightly lag the incoming sync pulse to prevent jitter of the HORIZCLK signal to U524B.

PHASE-LOCKED LOOP (PLL). Phase-Locked Loop U314 locks onto the horizontal-sync signal to produce a synchronized clock at twice the horizontal-sync rate (2XH). The 2XH clock is used to extract the various sync- and field-identification signals from the composite-sync waveform. It is also divided and delayed to obtain the DLY'D HCLK (see Figure 3-13) signal used in eliminating alternate equalizing and serration pulses from the HORIZCLK signal and the input to the PLL Phase Comparator inputs.

The 2XH VCO (voltage-controlled oscillator) output is divided by two by flip-flop U220B to produce both the HCLK and $\overline{\text{HORIZCLK}}$ signals at the horizontal-line rate. Horizontal sync from the input signal is applied to the Phase Comparator input of U314 at pin 14 via U308B. The $\overline{\text{HORIZCLK}}$ from the $\overline{\text{Q}}$ output of U220B is applied to U314 at pin 3 through U308C.

Phase Comparator output 2 (PC2 OUT at pin 13) of PLL U314, outputs the PLL ERROR signal whenever the leading edges of the $\overline{\text{HORIZCLK}}$ signal on pin 3 and the horizontal-sync pulses on pin 14 do not coincide. The error signal output is integrated by R322, R320, and C322 to produce a voltage (applied to pin 9) used to correct the operating frequency of the VCO. When either no phase errors exist or no signals are present to compare (both phase-comparator inputs at the same level), pin 13 goes to a high-impedance state, and the voltage on C322 maintains the operating frequency of the VCO. Resistors R323 and R324 and capacitor C324 set the operating frequency range of the PLL circuit. A bleeder resistor, R327, reduces the charge on C322 slightly between each error signal output so that the $\overline{\text{HORIZCLK}}$ signal will always lag the horizontal-sync of the input signal by a small amount. This

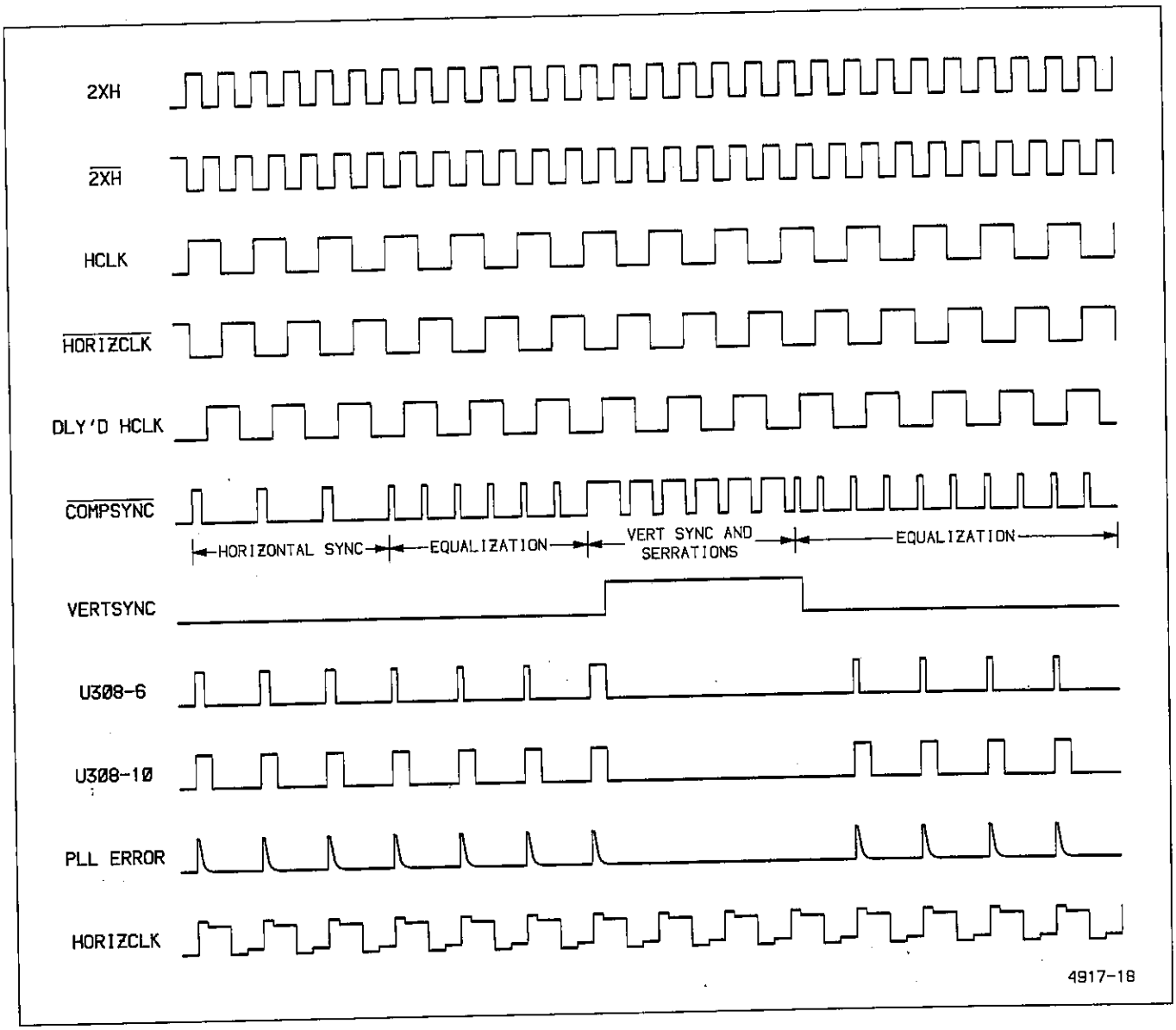


Figure 3-13. Video Option waveforms.

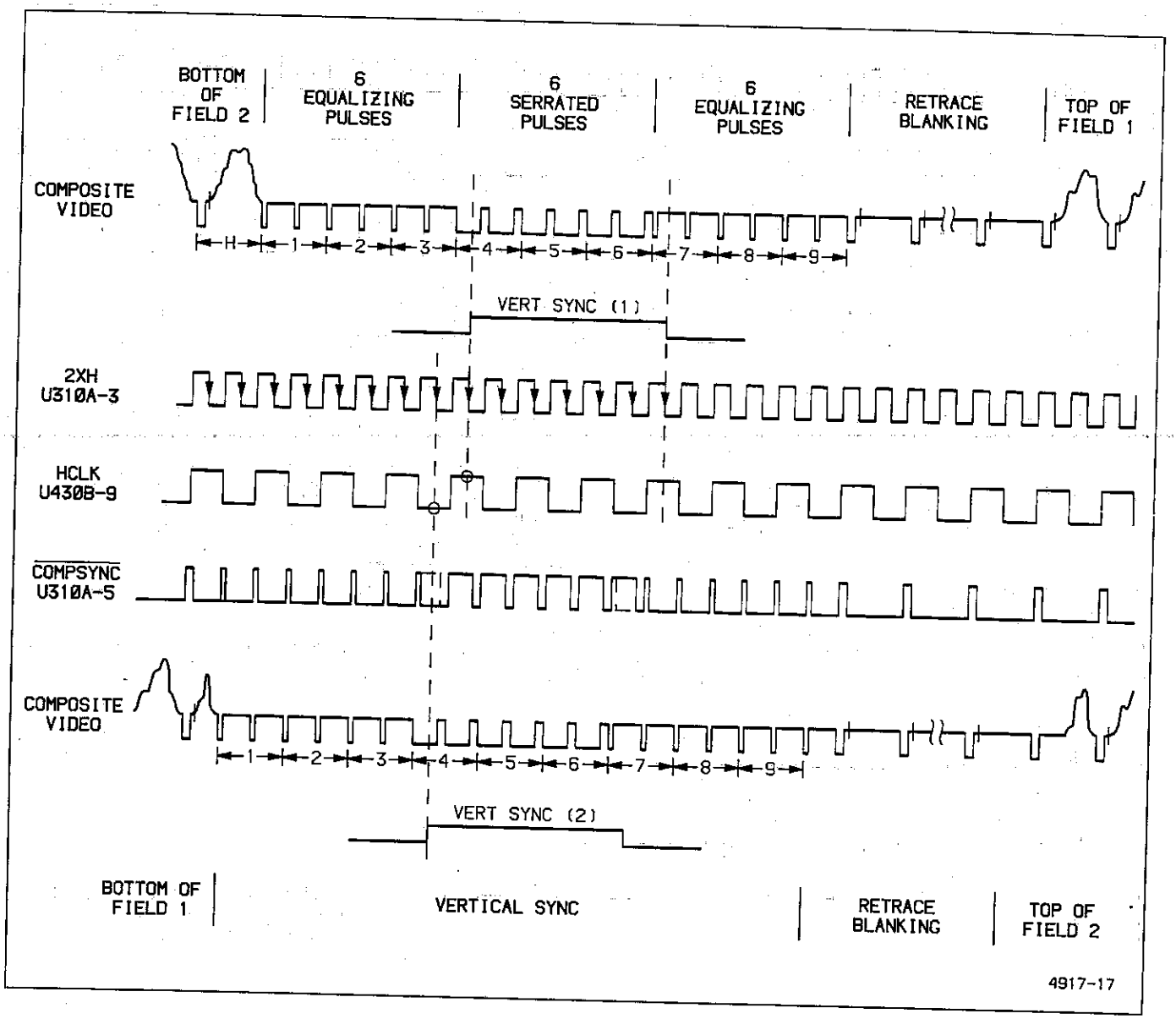


Figure 3-14. Video Option field-sync identification.

slight lag prevents the possibility of jitter in the HORIZCLK signal going to clock TV Trigger flip-flop U524B.

A similar signal (PLL LOCK) from pin 1 of the Phase Comparator is integrated by R326 and C330. If the PLL is not locked onto the input signal, the PLL LOCK output remains in the LO state long enough to be sensed by the PLL Unlock Detector. The long LO state of the PLL LOCK signal discharges C330 negative enough with respect to the emitter voltage of Q330, that the transistor becomes biased on. The collector voltage of Q330 will then go high, and Vertical Sync flip-flop U310A and Delayed Horizontal Clock flip-flop U220A will both be reset by the HI UNLOCKED signal. With U220A and U310A both reset, the DLY'D HCLK and VERTSYNC signals are held LO, and the equalizing pulses and vertical-sync serrations are no longer prevented from passing through NOR-gate U308B. The PLL Phase Comparator then sees the entire input signal during attempts to lock on so that locking will occur in the proper range. While the unlocked condition exists, the Channel 2 Vertical Display Clamp circuit is held disabled (via R328) by the HI state of $\overline{\text{TVCLAMP}}$ to prevent an invalid offset from being sent to the Channel 2 Vertical Preamplifier.

When lock is achieved, the phase difference between the two input signals becomes very small. The PLL LOCK pulse output level remains in the HI state (no error) long enough that C330 is allowed to charge positive and turn off transistor Q330. UNLOCK then goes LO to remove the resets from flip-flops U310A and U220A, allowing them operate, and $\overline{\text{TVCLAMP}}$ goes LO to enable the Channel 2 Vertical Display Clamp circuit. Unwanted equalizing pulses and the vertical-sync serrations are now prevented from passing to PLL Phase Comparator inputs by the DLY'D HCLK (delayed horizontal clock) and VERTSYNC signals applied to the PLL Phase Comparator Input NOR-gates, U308B and U308C (see Figure 3-13).

The DLY'D HCLK is shifted one-quarter HCLK cycle. When the DLY'D HCLK is HI, the outputs of both NOR-gates at the inputs to the PLL Phase Comparator are held LO, and the alternate equalizing pulses of composite-sync signal are prevented from passing to the PLL Phase Comparator. The vertical-sync serrations are prevented from passing through NOR-gate U308B by the HI VERTSYNC signal applied during vertical-sync times. Both types of unwanted pulses are thereby eliminated from the Phase Comparator inputs. The remaining sync pulses to be compared with the $\overline{\text{HORIZCLK}}$ signal are then only at the horizontal-sync frequency, and the VCO output frequency shifts slightly as necessary to bring that frequency to precisely twice the horizontal-sync rate (2XH). The charge on capacitor C322 holds the VCO to that output frequency throughout the vertical-sync period when all serration pulses are disabled from the Phase Comparator input and no comparisons are being made.

DELAYED HORIZONTAL CLOCK. The Delayed Horizontal Clock (DLY'D HCLK) is used to remove alternate equalizing pulses and serration pulses from the composite-sync waveform in order to maintain precise sync for horizontal line counting. The PLL-generated HCLK signal from the Q output of U220B is clocked into U220A by the $\overline{\text{2XH}}$ pulse from NOR-gate U308A (acting as an inverter). The inversion of the two-times clock delays the Q output of flip-flop U220A by one-quarter of a horizontal clock (HCLK) cycle. The quarter-cycle delay enables the HI portion of the output (applied to U420B via R210) to mask the alternate, unwanted equalization and serration pulses (occurring at twice the horizontal-sync rate) from the HORIZCLK output by preventing U420B, in the Pulse Stretcher circuit, from switching during those time periods. The same signal masks the unwanted equalization pulses from the PLL inputs by disabling NOR-gates U308B and U308C from passing signals to compare during the DLY'D HCLK HI state. All the vertical-sync serration pulses are eliminated from the PLL Phase Comparator input by the HI state of the VERTSYNC signal applied to the input NOR-gates.

VERTICAL SYNC. The Vertical Sync circuitry outputs pulses for both the Field 1 and the Field 2 vertical-sync times. These VERTSYNC pulses are used to toggle the Field Sync Generator. The VERTSYNC signal is produced by clocking the level of the $\overline{\text{COMPSYNC}}$ signal on the D input (pin 5) of U310A into that flip-flop using the inverted two-times horizontal clock $\overline{\text{2XH}}$. Figure 3-14 shows that only during a vertical-sync interval will the $\overline{\text{COMPSYNC}}$ signal be HI on the rising edge of the $\overline{\text{2XH}}$ clock. At all other (non-vertical sync) times, the $\overline{\text{COMPSYNC}}$ signal will be LO on the rising edge of the 2XH clock. Thus, the Q output of flip-flop U310A will be clocked HI during vertical-sync intervals for VERTSYNC, and it will be clocked LO during the rest of the field.

FIELD-SYNC GENERATOR. The Field-Sync Generator produces the FIELD signal used in identifying the individual fields of picture information. For interlaced-scan signals, the signal identifies which field a given line of picture information belongs to (exceptions are explained in the Line Counter description); while, for non-interlaced-scan signals, it toggles to indicate vertical sync. The circuit consists of an Interlace/non-Interlace Detector, a Vertical-Sync Latch (interlaced), and a Vertical-Sync flip-flop (non-interlaced).

To detect whether a signal is interlaced (two vertical-sync pulses per frame) or non-interlaced (only one vertical-sync pulse per frame), flip-flop U310B is clocked to transfer the level of the HCLK signal on the D input to the $\overline{\text{Q}}$ output by the VERTSYNC clock at the start of a vertical-sync period. For non-interlaced displays, the

vertical-sync rising edge always occurs during a HI portion of the HCLK signal, and the $\overline{Q}$ output of U310B will be clocked HI; while, for interlaced displays, the $\overline{Q}$ output will alternate between HI and LO.

The $\overline{Q}$ from pin 12 of U310B controls two other flip-flops U430A and U430B, through the circuit action of transistors U420A and Q422. If the output of U310B is not toggling (non-interlaced signals), transistor U420A will be turned off by pull-down resistor R426. This allows the base bias voltage of Q422 to go positive as C426 charges through R429 and R428. Soon, Q422 is biased off and flip-flop U430B becomes reset. The reset on U430B from C426 holds the $\overline{Q}$ output HI to reverse bias CR334 and isolate the $\overline{Q}$ output from the FIELD signal line. At the same time, the LO TVINTERLACED signal applied to the set input of U430A from the collector of Q422 enables that flip-flop to toggle on the rising edges of the vertical-sync pulses applied to the clock input (pin 3). This toggling is required to reinitialize the counters after they have counted their last lines. The TVINTERLACED signal is also applied to the Processor Miscellaneous Buffer (U854, diagram 1) where it may be read by the System μP to determine whether the video signal is interlaced or non-interlaced. The System μP must be able to determine this information to properly control the line counting.

For interlaced displays, the output from U310B will toggle. This will alternately turn transistor U420A on and off at the vertical-field rate. The first time U420A gets turned on by an interlaced-system signal, it discharges C426 and turns Q422 on. Capacitor C426 will charge positive through R429 and R428 when U420A turns off, but the long time constant of the charging path prevents the charge from getting positive enough to reassert the reset to U430B before the next toggle cycle once again discharges the capacitor. Flip-flop U430A is held set by the HI TVINTERLACED (interlaced) signal asserted from the collector of Q422, and CR336 is reverse biased to isolate U430A from the FIELD signal line. The resulting FIELD signal, as a result of the output of flip-flop U430B, will be HI for all lines in Field 1 and LO for all lines in Field 2 (with a few exceptions that are explained in the Line Counters description).

LINE COUNTERS. Line Counter U530 contains three programmable counters (at decoded addresses 6808h through 680Fh) that are set by the System Processor to determine when the chosen line number in the field selected for triggering is reached. The various control registers of the counter are set up to count horizontal clock pulses (lines) to determine line location in the field.

The Line Counter is enabled whenever its address block is decoded by the system Address Decode circuitry. To differentiate it from the GPIB circuitry (which also answers for the same block of decoded addresses), the Video Option uses address bit A3 as a second chip select. Specific registers within the Line Counter are addressed using address lines A0-A2 applied to the register-select inputs. Reading and writing of the selected register is controlled by the System μP using the $\overline{WR}$ select line while the E (enable) clock synchronizes transfers to the System μP rate.

Once the proper setup data (defining counter mode and line number) is written to the Line Counter, the enabled counter will begin counting horizontal clock pulses (lines). Counters are alternately started as the FIELD signal toggles, and counters 1 and 2 produce a LO output when their predefined counts are reached. Counter 3 is used to determine the number of LINES in a FIELD (of FIELD 2 if in an interlaced system). The System μP checks the "previous field" line count by reading the counter contents via the data bus.

LINE COUNT ADJUSTMENTS. Depending on the type of signal being triggered upon (System M or non-System M) and the desired line for trigger, the System μP adjusts both the numbers preloaded to the counters and the field to which the assigned line-count relates. These line-count and relative-field adjustments are required for the following reasons.

1. The HORIZCLK coincident with a switch in the FIELD indicator does not produce a count. Since the FIELD change doesn't enable the opposite counter in time to catch the rising edge of the HORIZCLK (responsible for the change), the preloaded line count must be reduced by one.

2. The counters cannot produce a "zero-count" delay; i.e., the counter output goes LO one count (line) after the counter reaches zero. Even when set to zero, a count must still occur; so the line count must be reduced by one again.

3. The counter outputs merely arm the trigger circuit, with the next line sync producing the actual trigger; therefore, line count must be reduced again by one.

RELATIVE FIELD ADJUSTMENTS. For non-System M television signals (line one coincident with the FIELD sync pulse), the line-adjustment requirements described above require that the first three lines of either field be counted relative to the previous FIELD pulse.

Since, by definition, System-M fields begin numbering lines three lines before the vertical field-sync occurs, and due to the line-adjustment requirements described above, the first six lines of System-M fields must be counted relative to the previous FIELD pulse.

As stated in the "Line Count Adjustments," the trigger arming pulse occurs one line count prior to reaching the selected trigger line. Depending on whether the System Processor has selected the arming pulse relative to Field 1 or Field 2, either NAND-gate U541C or NAND-gate U541D will be enabled by a control bit (FLD1 or FLD2) from Video Option Control Register U750. The selected pulse, when it occurs, is passed through the enabled gate, through U541A and U424D, and appears as a clock pulse at the trigger-arm flip-flop, U524A.

TV TRIGGER GENERATOR. The TV Trigger Generator circuit produces the signal to trigger the Oscilloscope at the designated horizontal line. The output from the Line Counter arms the TV Trigger Generator circuit, enabling a trigger to be produced on the next line-sync pulse. Generation of a TV trigger from the circuit is enabled by a HI TVENA (TV-enable) bit from Video Option Control Register U750 (diagram 20).

In the Video Option, as in the main Trigger Generator a trigger signal is inhibited from being produced during trigger holdoff. For the holdoff period, the ATHO (A-trigger holdoff) signal applied to U424C is HI to hold arming flip-flop U524A reset which, in turn, holds trigger flip-flop U524A reset. When the holdoff processing cycle is completed, the ATHO signal goes LO to remove the reset from U524A and enable triggering.

Assuming TV Line Coupling mode is not active, the LINECPL (line coupling) bit applied to U541B pin 5 will be LO, and arming flip-flop U524A will be enabled. When the Line Counter has counted the proper number of lines relative to the Processor-selected field, flip-flop U524A will be clocked. This produces a HI "armed" level applied to the reset input of trigger flip-flop U524A that releases the reset condition of the flip-flop. The next HORIZCLK pulse (line) then clocks a LO to the $\overline{Q}$ output, $\overline{TVTG}$, that defines the trigger point in the acquisition record. The $\overline{TVTG}$ output is reset HI when trigger holdoff (ATHO) goes HI to reset the flip-flop via U424C and U524A.

When TV Line Coupling mode is selected, the LINECPL bit from the Video Option Control Register will be set HI. This causes flip-flop U524A to be immediately armed when A trigger holdoff ends by forcing a set signal to pin 4 of that flip-flop through NAND-gate U541B. In this mode, a trigger will occur on the first line sync following the end of each holdoff interval. The resulting display will be stable with respect to horizontal sync pulses but will not be stable with respect to the vertical sync pulses.

CH2 VERTICAL DISPLAY CLAMP. The Channel 2 Display Clamp circuit clamps the back-porch level of the triggered-display signal near the on-screen zero-volt reference. This allows automatic positioning of the display on the crt when probing various points with differing dc levels and removes vertical jitter that would be caused by 60-Hz hum riding on the television signal.

The Channel 2 Pickoff (CH2 PO) signal from the Channel 2 Preamplifier is applied through a low-pass filter formed by R524 and C514. The filter removes all the high-frequency components from the composite video signal, but its purpose is to specifically remove the color-burst modulation from the back-porch of the sync pulses. The filtered sync pulse is then amplified with respect to ground during its back-porch interval either by operational amplifier U514 or by operational amplifier U520, depending on the display polarity chosen by the operator. The selected comparator, when gated on (via U410A and either R410 or R411) during the back-porch interval, produces a dc-offset voltage used to shift the back-porch level of the displayed channel 2 signal to zero volts. Capacitor C522 acts as a hold capacitor to maintain a constant dc offset to the Channel 2 Vertical Preamplifier between back-porch samples. Operational amplifier U710D buffers the offset signal to the Channel 2 Preamplifier.

Offset gain of Channel 2 Preamplifier U320 is set higher when the CH2 VOLTS/DIV switch is set to 2 mV, 5 mV, 10 mV, 100 mV, or 1 V/Div. At those VOLTS/DIV settings, the FASTCLAMP bit is set LO to turn on U420E. This turns FET Q419 on and places C520 in parallel with C522 thus increasing the size of the hold capacitance. This slows down the loop response at the "more sensitive" offset gain setting of the Channel 2 Preamplifier to prevent oscillation.

CLAMP SWITCHING. The Clamp Switching circuit enables and disables the effect of the Channel 2 Vertical Display Clamp. The clamp circuit operation may be switched to provide correct clamping for either inverted or noninverted video signals.

When display clamping of the Channel 2 signal is not enabled, BCLAMPENA will be set LO, turning U420D on. The HI on the collector of U420D turns on U410B, U410C, and Q420 and turns off Q710 via U710A. Any enabling currents to offset amplifiers U514 or U520 are shunted through U410B and U410C respectively. With FET Q420 on, the input to U710D will be grounded. This disables the

Offset Buffer. With FET Q710 turned off via U710A, the offset line to the Channel 2 Vertical Preamplifier is open circuited, so no trace offsetting can occur.

When the Channel 2 Vertical Display Clamp is enabled, BCLAMPENA will be HI, turning U420D off. The LO on the collector of U420D turns Q420 off, enabling Offset Buffer Amplifier U710D to track the offset level output from the active Offset Amplifier, and the offset signal line to the Channel 2 Vertical Preamplifier is connected to the Offset Buffer by turning on Q710 via U710A.

Selection of either U514 or U520 is controlled by the CH2 INV signal and is dependent on the setting of the invert function in the associated COUPLING/INVERT menu. Since signal offsetting in the Channel 2 Preamplifier is done before the signal is inverted, offset voltages for inverted- and normal-signal displays must be of opposite polarity. Switching between these two offset amplifiers provides the required polarity change and allows the back porch of either display type to be clamped at the ground reference. Depending on the polarity of the CH2 INV (Channel 2 Invert) signal, either U410E or U410D will be on, turning off either U410B or U410C. U410B will be off when CH2 INV is HI and U410C will be off when it is LO. Bias current from the Trigger Back-Porch Clamp circuit to the offset amplifiers (U514 and U520) is not shunted away by the "off" transistor, and the offset amplifier associated with the off transistor will be biased on during the sync pulse back-porch interval.

Biasing current to enable the selected Offset Amplifier is produced during the back-porch interval when U410A (in the Trigger Back-Porch Clamp circuit) is turned off. Bias current through either R411 or R410 (depending on whether U410B or U410C is off) is supplied via R403. The other offset amplifier will be disabled since its bias current is being shunted through the "on" transistor. The amount of bias current permitted by Transconductance Amplifier U504 to the "on" amplifier provides a signal to the Channel 2 Preamplifier (after buffering by U710D) that vertically offsets the displayed signal on Channel 2.

Since the offset voltage must be maintained throughout the entire horizontal interval, capacitor C522 (and C520 in parallel if FASTCLAMP is not enabled) serves as a hold capacitor between back-porch samples. At some VOLTS/DIV settings the Channel 2 Preamplifier is set for higher offset gain. Transistor Q419 will be turned on for those settings, placing C520 in parallel with C522 to slow down the loop response. This prevents oscillation in the Channel 2 Preamplifier at the more sensitive gain settings.

Offset Buffer Amplifier U710D applies this "stored" offset level to the Channel 2 Preamplifier (via Q710), shifting the back porch of the displayed signal to near the on-screen ground reference (as set with the Vertical POSITION control).

Any time the Phase-Locked Loop is not locked (indicating that a proper TV Trigger signal is not present), the Channel 2 Vertical Display Clamp is turned off via R328 by a HI $\overline{\text{TVCLAMP}}$ signal from the PLL Unlock Detector to prevent sending invalid offsets to the Channel 2 Preamplifier. During the unlocked state of the PLL, FET Q420 is biased on to pull the input to Offset Buffer Amplifier U710D to ground, and FET Q710 is biased off via U710A (acting as an inverter to the $\overline{\text{TVCLAMP}}$ signal) to open circuit the offset signal line to the Channel 2 Preamplifier.

LOW-VOLTAGE POWER SUPPLY

The low voltages required by the scope are produced by a high-efficiency, switching power supply (diagram 22). This type of supply directly rectifies and stores charge from the ac line supply; then the stored charge is switched through a special transformer at a high rate, generating the various supply voltages.

AC Power Input

LINE SWITCHING AND LINE RECTIFIER. Ac line voltages of either 115 V or 230 V may provide the primary power for the instrument, depending on the setting of the LINE VOLTAGE SELECTOR switch S1000 (located on the instrument rear panel). POWER Switch S1350 applies the selected line voltage to the power supply rectifier (CR510).

With the selector switch in the 115 V position, the rectifier and storage capacitors C105 and C305 operate as a full-wave voltage doubler. When operating in this configuration, each capacitor is charged on opposite half cycles of the ac input, and the voltages across the two capacitors in series approximates the peak-to-peak values of the source voltage. For 230 V operation, switch S1000 connects the rectifier as a conventional bridge rectifier. Both capacitors charge on both input half cycles, and the voltage across C105 and C305 in series approximates the peak value of the rectified source voltage. For either configuration (with proper line voltage), the dc voltage supplied to the power supply inverter is the same.

SURGE PROTECTION. Thermistors RT717 and RT805 limit the surge current when the power supply is first turned on. As current warms the thermistors, their resistances decrease and have little effect on circuit operation.

Spark-gap electrodes E609 and E616 are surge voltage protectors. If excessive source voltage is applied to the instrument, the spark-gaps conduct, and the extra current quickly exceeds the rating of F1000. The fuse then opens to protect the power supply.

EMI FILTER. A sealed line filter, FL1000, is packaged with the line cord connector. It is effective in reducing noise with frequency components at and beyond 1 MHz. A differential mode filter is made up of R809, C816, R815, L715, L709, R808, R713, and C706 and is effective in reducing switch-mode noise up to 1 MHz. Resistor R1000 ensures that the capacitors in the line filter become discharged a short time after removal of the line cord so as to not present a shock hazard at the line cord connector. A combination common-mode and differential-mode filter is made up of T117, R217, R117, C218, C225, and C328. The line-rectification energy-storage capacitors (C105 and C305) also aid in the operation of this filter circuit. Resistors R410 and R401 bleed charge from the line-rectification capacitors to guarantee that they are discharged within a definite time after power is removed (turned off).

THERMAL SWITCH. Thermal Switch S1020 opens if the temperature of the power supply heatsink becomes abnormally high. High temperatures may indicate blocked ventilation holes or failed components. Opening the switch removes ac-line power from the supply to prevent any further damage from occurring. When the heatsink cools to its normal limits, the switch recloses. Opening of S1020 immediately shuts off the power supply, and the System μP does not perform its normal shutdown routine. Waveforms and front-panel settings are not saved on a thermal shutdown.

Control Power Supply

The control circuits for the power supply require a separate power supply circuit to operate. This independent power source is made up of Q148, Q240, Q836, and associated components.

Initially, when instrument power is applied, the positive plate of capacitor C244 is charged toward the value of the positive rectified-line voltage through R223. The voltage at the base of Q148 follows at a level determined by the voltage divider composed of R436, R244, CR239, R240, R640, Q836 and the load resistance placed on the supply. When the voltage across C244 reaches about +27 V, the base voltage of Q148 reaches +12.6 V and Q148 turns on, saturating Q240. The +27 V on the emitter of Q240 appears at its collector and establishes the positive voltage supply for the +12 V regulator stage formed by Q836, VR929, R240, and R640. With Q240 on, R244 is placed in parallel with R436 and both Q148 and Q240 remain saturated.

The +27 V level begins to drain down as the +12 V Regulator draws charge from C244. If the main power supply doesn't start (and thus recharge C244 via T335 and CR245) by the time the voltage across C244 reaches about +14 V, Q240 turns off. With Q240 off, resistor R244 pulls the base of Q148 low and turns it off also. (Capacitor C244 would only discharge low enough to turn off the transistors under a fault condition.) In this event, C244 would then charge again to +27 V, and the start sequence would repeat. Normally, the main power converter is delivering adequate power before the +14 V level is reached, and the current drawn through T335 via Q421 and Q423 induces a current in the secondary winding of T335 that charges C244 positive via diode CR245. The turns ratio of T335 sets the secondary voltage to approximately +17 V and, as long as the supply is being properly regulated, C244 is charged to that level and held there.

Power Conversion

The power converter consists of a buck-type switching Preregulator, producing width-regulated voltage pulses that are filtered to produce a preregulated dc current, and an Inverter stage that chops this preregulated current into ac to drive a power transformer. The transformer has output windings that provide multiple unregulated dc voltages after rectification has taken place. The main Preregulator components are Q421, Q423, CR426, C328, T335, T620, and U233. The fundamental Inverter components are Q521, Q721, T639, and U829B (see Figure 3-15).

PREREGULATOR. The Preregulator control circuit monitors the drive voltage reflected from the secondary to the primary of the Inverter output transformer T639 and holds it at the level that produces proper supply voltages at each of the secondary windings.

The Preregulator control circuit consists primarily of control IC U233, gate drive transformer T620, and the associated bias and feedback circuit elements. The voltage at the primary center tap of T639 is attenuated and applied to the voltage-sense input of control IC U233. This IC varies the "on time" of a series switch, depending on whether the sensed voltage is too high or too low. Transistors Q421 and Q423 form this "series switch," and are each active during alternate switching cycles. The on-time duty cycle of the series switch is inversely proportional to the rectified line voltage on C328. In normal operation, the series switch is on about one-half of the time. When the series switch is off, current to T639 is through CR426.

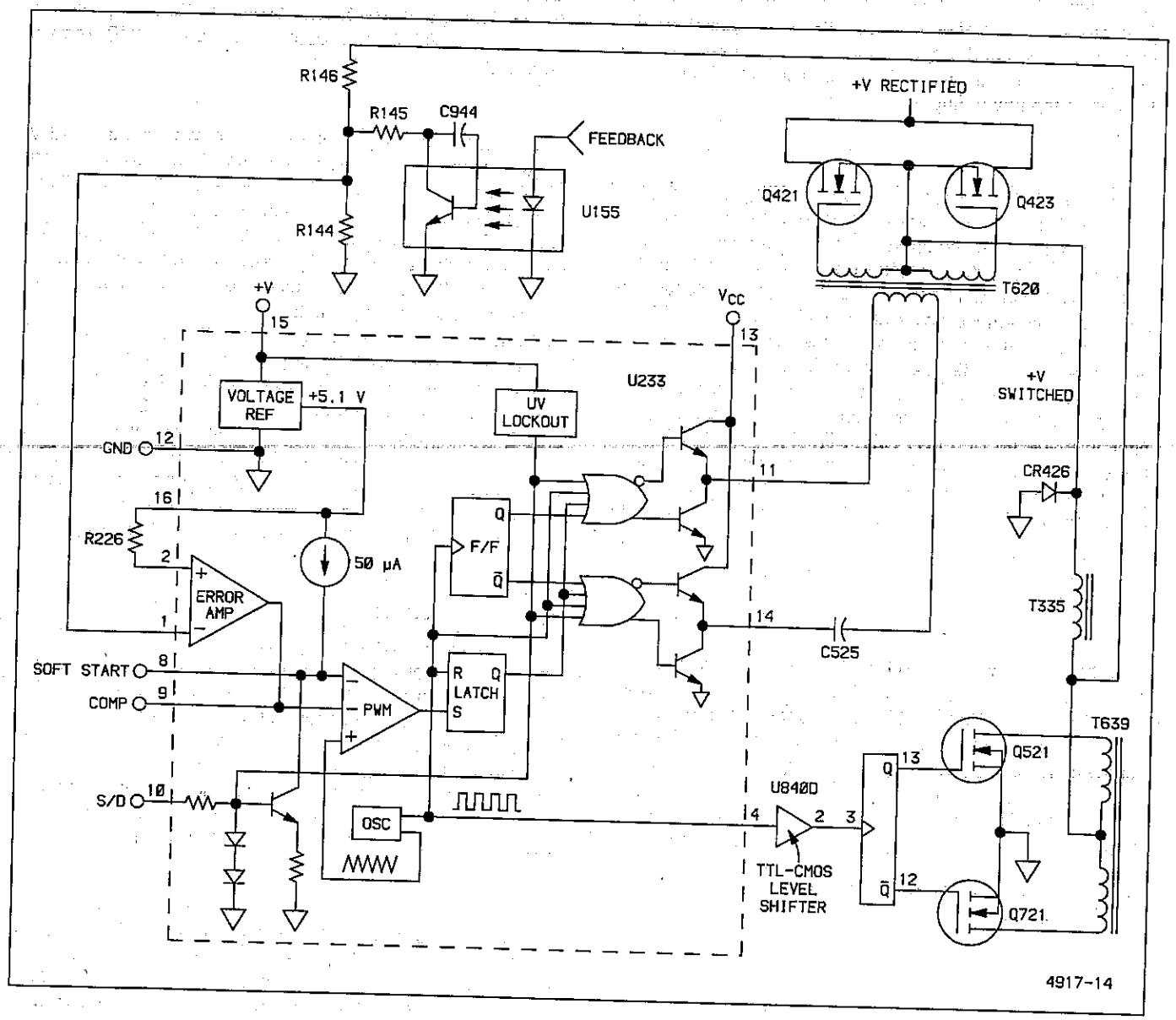


Figure 3-15. PWM Regulator and Inverter.

PREREGULATOR START-UP. As the supply for the Preregulator control IC is established, an internal oscillator begins to run. The oscillator generates a repetitive triangular wave (as shown in Figure 3-16) at a frequency determined primarily by R228 and C227 (with R227 having a minor effect since it controls the discharge time of timing capacitor C227).

As the control power supply turns on, a 50 μA current source internal to U233 begins to charge capacitor C128 positive. This charging level, applied to one of the negative inputs of the PWM comparator, allows drive pulses of greater and greater duty cycle to be generated. These pulses drive the series switching transistors (Q421 and Q423), and their slow progression from narrow to wide causes the various secondary supplies to gradually build up to their final operating levels. This slow buildup prevents a turn-on current surge that would cause the current-limit circuitry to shut down the supply.

PREREGULATION. Once the initial charging at power-up is accomplished (as just described), the voltage-sensing circuitry begins controlling the Inverter switching action. The voltage level at the primary center tap of T639 is divided by sense string R146-R144, and the resulting voltage is applied to the error amplifier internal to U233 at pin 1. The +5.1 V reference generated by U233 is applied to pin 2 of U233, the other input of the error amplifier. If the sensed level at pin 1 is lower than the reference level at pin 2 (as it always is for the first few switching cycles), the output of the error amplifier is high. This high level is applied to a negative input of the PWM comparator; the other negative input is applied from the soft-start capacitor (described previously).

The lower of the two negative input levels determines the actual negative comparison point of the PWM comparator; and this level determines the point at which the positive-going ramp, applied to the positive input, switches the PWM comparator to initiate the off state of the PWM switch. The PWM series switch is turned on at the beginning of each clock cycle; turn-off occurs when the positive-going ramp crosses the threshold level of the PWM comparator. The lower the level at the controlling (negative) input, the shorter the PWM switch "on time." Depending on the output level sensed, the duty cycle of the drive signal changes (sensed level rises or falls with respect to the triangular waveform applied to the positive PWM comparator input) to hold the secondary supplies at their proper levels.

Optoisolator U155 and resistor R143 form a control network that allows a voltage sensed at the FEEDBACK input to slightly alter the voltage-sense reference applied to pin 1 of U233. The FEEDBACK signal is generated by the +5 V Inverter Feedback amplifier (U189, diagram 23) and is directly related to the level of the +5 VD supply line. If the FEEDBACK signal goes above its nominal level (+5 VD is too low), base drive to the shunt transistor (in optoisolator U155) increases. This increase causes additional current to be shunted around R144 (via R143 and phototransistor of U155) and changes the ratio of the sensing divider. The voltage at the center tap of T639 must increase to balance out the changed sense ratio and maintain balance in the error amplifier. Since the output of the error amplifier controls the current to the primary winding of the output transformer, and since the error amplifier sensing depends on a balanced condition, the voltage at the transformer primary increases.

With a higher current applied to the transformer primary, higher voltages appear across the secondary windings of T639 with each cycle. This causes the secondary voltages to return to their nominal levels. As the +5 V_D line returns to its nominal level, base drive to the shunt transistor stabilizes at a level that keeps the sensed +5 V_D level in regulation. Should the FEEDBACK signal level tend too high, opposite control responses occur. Further information about the FEEDBACK signal is given in the +5 V Inverter Feedback description.

INVERTER. The Inverter circuit alternately switches current through each leg of the primary winding of output transformer T639. The circuit is made up of Q521, Q721, U840D, U829B, and associated components.

A clock pulse from U233 is applied to a TTL-CMOS level shifting buffer (U840D) at the beginning of every switching cycle. The level-shifted clock pulse at the output of U840 clocks U829B, a CMOS D-type flip-flop (configured to toggle with each clock). The Inverter switch transistors, Q521 and Q721, are alternately turned on and off by the flip-flop outputs and are connected to opposite ends of the primary winding of the output transformer. Driving the inverter switches in alternate fashion produces ac currents in the secondary windings of the output transformer that are rectified, providing the various unregulated dc supply voltages.

Primary Fault Sensing

Primary current, primary regulated voltage, and primary unregulated voltage are monitored by circuitry to prevent catastrophic failure. Should conditions arise that cause an excessive primary current or an excessive primary regulated voltage, limiting occurs. The excessive primary current and primary regulated voltage functions share much common circuitry, while the low unregulated primary voltage circuitry is entirely independent of the first two fault-sensing circuits.

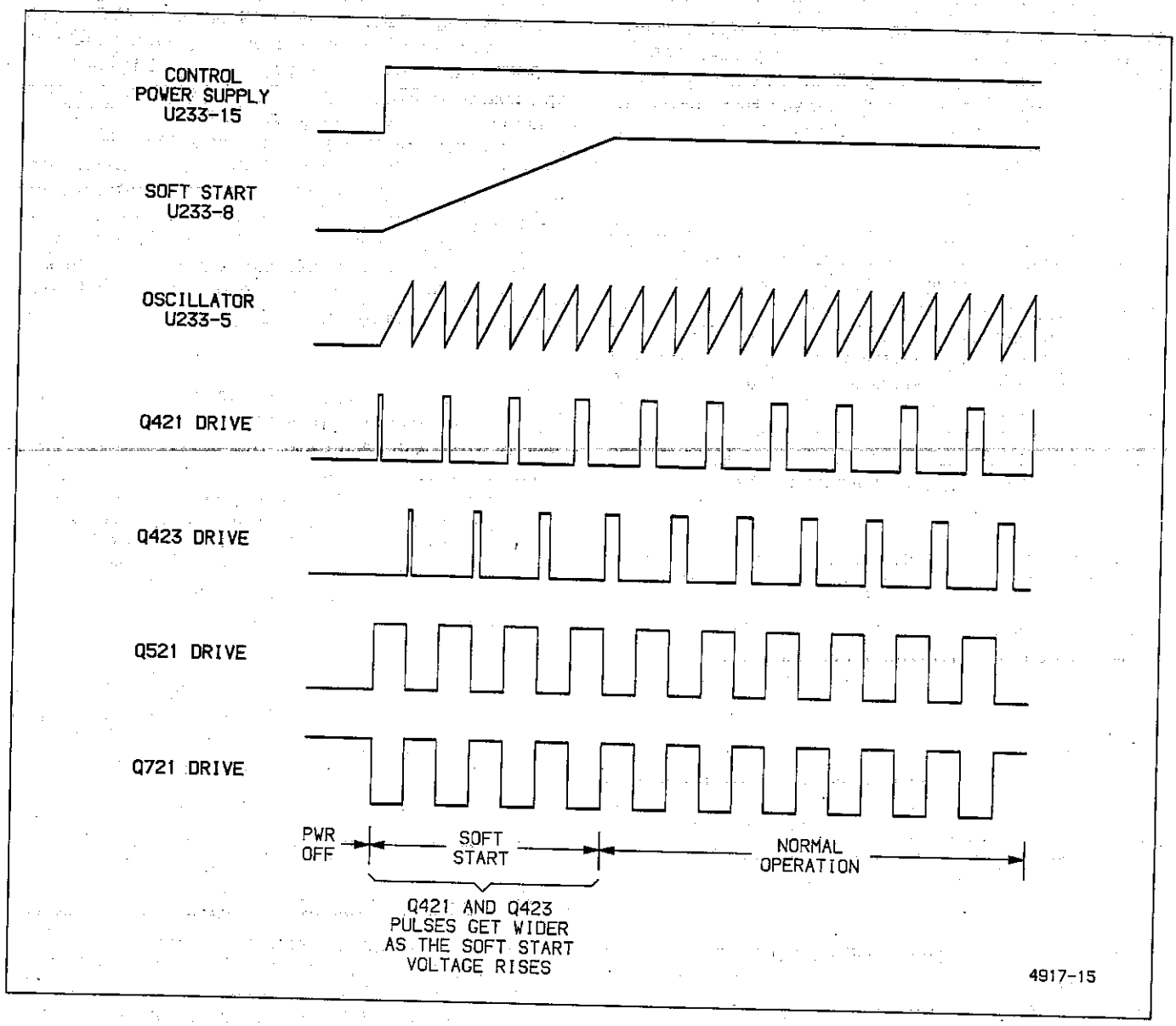


Figure 3-16. PWM switching waveforms.

PRIMARY OVER-CURRENT SENSING. The primary current of T639 through R727 produces a voltage signal that is filtered by R728 and C728 to remove high-frequency switching spikes. The filtered signal is applied to the inverting input of U840C. The noninverting input of the comparator is set at a level defined by the +5.1 V reference from U233 and voltage divider R939-R836. If an excessive-current condition exists (to the point that the inverting input of U840C goes more positive than the noninverting input), the comparator output goes low. The open-collector output of the comparator is "wire-ORed" with the open-collector output of the regulated primary over-voltage comparator (U840B) and drives U840A, connected as an inverting buffer. Buffer U840A drives the clock input of a CMOS flip-flop in U829, configured as a monostable flip-flop, used to shut down supply operation.

PRIMARY OVER-VOLTAGE SENSING. The regulated primary voltage is sensed by the voltage divider R129-R128, with C528 providing low-pass filtering to remove high-frequency switching spikes. The attenuated signal is applied to comparator U840B at the inverting input, while the noninverting input is connected to the +5.1 V reference from U233. Should the regulated primary voltage become high enough to raise the inverting input of the comparator more positive than the noninverting input, the comparator output goes to a low level. As previously stated, the output of this comparator is wire-ORed to the output of U840C and drives an inverting clock buffer U840A. This buffer in turn drives the clock input of the monostable flip-flop circuit used to shut down supply operation.

SHUTDOWN TIMER. The Shutdown Timer ensures that the preregulator series switch remains off long enough for energy stored in C128 (the soft-start capacitor) and C244 (the Control Power Supply energy-storage capacitor) to drain down via normal circuit loading should an over-current or over-voltage fault occur. Shutdown of the series switch (Q421 and Q423) occurs when the S/D (shutdown) input (pin 10) of U233 goes high. The Shutdown Timer, made up of U829A, R824, C829, R932, CR730, and CR824, controls this input.

Prior to being clocked, U829A (configured as a monostable flip-flop) is in a reset state with its Q output set low. This is the normal operating mode and allows the series switch to be controlled by the regulating functions of U233. Capacitor C829 charges to the Control Power Supply voltage via R824 and CR824 (diode CR824 shunts R932 when charging C829 to provide a relatively fast charging path). When the flip-flop is clocked (indicating a fault-sense from the voltage- or current-sense circuits), the Q output goes high and C829 begins to discharge. With Q high, CR824 becomes reverse biased so that discharge of C829 is through R932, providing a relatively slow discharge compared to the charging time. This ensures that the Q output of U829A is held high long enough for soft-start capacitor C128 and Control Power Supply capacitor C244 to fully discharge.

The high Q output of U829A, connected to the shutdown input to U233, turns off the PWM switch (Q421 and Q423) immediately and keeps it off until Q returns low (when the Control Power Supply decays and turns U829 off). However, the PWM clock continues to run and the Inverter switches (Q521 and Q721) continue to operate. Since the PWM switch is not operating, energy is not transferred to the Control Power Supply via T335, and C244 discharges below the minimum voltage level required by the Control Power Supply circuit (through the normal circuit load). When this minimum level is reached, the Control Power Supply regulator disconnects from C244, interrupting the power to the control circuitry and stopping the Inverter switches.

Monostable U829A is designed to remain active long enough for the Control Power supply to decay and disconnect. The disconnect level is approximately half of the Control Power Supply voltage and, once disconnected, supply voltage is reestablished in 0.5 to 2 seconds. The time it takes C244 to charge from the "disconnect threshold" to the Control Power Supply "turn-on threshold" is the dominate factor in determining the power supply restarting time when recovering from an over-current or over-voltage fault condition.

Capacitor C829 is once again charged through R824 and CR824 with a relatively short time constant, allowing U829A to be triggered again (if the fault persists) by the time the Control Power Supply restarts.

LINE UP. The Line Up circuit, composed of U834B, U265, and associated components, senses the level of the rectified line voltage and relays its status through the PWRUP circuit to the System μP. The signal from voltage divider R325-R835 is low-pass filtered by C835 and is applied to the inverting input of comparator U834B. The noninverting input of the comparator is referenced to the +5.1 V reference from U233. The output of the comparator drives the light-emitting diode of optoisolator U265, so whenever the rectified line-input voltage is below the normal operating level (approximately +178 V), the light-emitting diode (LED) is off. With the LED off, the output phototransistor of U265 is biased off.

At instrument turn-on, after the rectified line voltage comes up, the control power supply begins supplying power to the control circuitry. At that time, the output of comparator U834 goes LO at pin 7 to turn on the LED in optoisolator U265. This action biases on the output transistor of the optoisolator and switches the LINE UP

signal HI. Through the PWRUP signal circuitry, a HI LINE UP signal tells the System μP that ample line voltage is available for normal instrument operation.

When instrument power is turned off, the rectified line voltage begins dropping. At about 178 V, comparator U834 switches off the LED in U264, and the LINE UP signal goes LO. A LO output tells the System μP that power is dropping, and the μP begins shutting the instrument down in an orderly fashion before the secondary voltages go out of regulation.

Line Trigger

The Line Trigger circuit, made up of T415, U170A, and the associated components, provides a representation of the input line signal to the Trigger stage that is isolated from the power-line environment.

Since resistors R516 and R518 are large compared to the impedance of the primary winding in T415, the transformer operates in a current-driven mode. The secondary winding of T415 is connected to a transresistance amplifier stage consisting of U170A, C483, and R483. This amplifier presents a very low impedance to the output of the transformer and maintains the integrity of the line voltage signal representation. Capacitor C483 provides a negative-feedback path to high frequencies (relative to 60 Hz) and reduces noise on the line-frequency signal. The output of the transresistance amplifier drives the oscilloscope trigger circuitry.

Rectifiers

The Rectifiers convert the alternating currents from the secondary windings of the Inverter output transformer to the various unregulated dc voltages required by the instrument. Rectification is done by conventional diode rectifier circuits, and filtering is done by conventional LC networks.

LOW-VOLTAGE REGULATORS

The Low-Voltage Regulators (diagram 23) remove ac voltage noise and ripple from the various unregulated dc supply voltages. Each regulator output is automatically current limited if the output current exceeds the requirements of a normally functioning instrument. This limiting prevents any further component damage.

+10 V and −5 V References

Each of the power supply regulators controls its respective output by comparing the output voltage to a known reference level. In order to maintain a stable supply voltage, the reference voltage must itself be highly stable. The circuit composed of U180, U170B, U900, and associated components produces the two reference levels used by the regulator circuits.

Resistor R556 and capacitor C664 form an RC filter network that smooths the unregulated +15 V_A supply before it is applied to voltage-reference IC U180. The +10 volt output from pin 6 of U180 feeds a low-pass filter composed of R900 and C900. The output of this filter in turn feeds unity-gain buffer amplifier U900, the output of which is the source of the +10 V reference used by the various positive regulators. Low-pass filter R900-C900 provides filtering for the IC voltage reference and provides for a well-defined voltage rise of the +10 V_{REF} voltage at power-up.

Operational amplifier U170B and its associated components make up a −5 V Reference circuit used as the reference for the negative regulators. It is configured as an inverting amplifier with a gain of 1/2 and converts the +10 V_{REF} input to a precision −5 V_{REF} output.

+15 V Regulator

The +15 V Regulator uses three-terminal regulator U579 and operational amplifier U570A (arranged as the voltage sensor) to achieve regulation of the +15 V supply). The three-terminal regulator holds its output voltage on pin 2 at 1.25 V more positive than the reference input level applied to pin 1. The voltage at the reference pin is established by current in diode CR575 and is controlled by voltage sensor U570A.

Resistors R576 and R575 at the regulator output divide the +15 V level down for comparison to the +10 V reference applied to pin 3 of operational amplifier U570A. At initial power up, when the input voltage at pin 2 (from the divider) is lower than the +10 V reference, the output of amplifier U570A is high, and the output voltage is allowed to rise. As the regulator output reaches +15 V, the amplifier begins sinking current away from the reference pin of the three-terminal regulator via diode CR575. This sets the voltage on the reference pin at its nominal level and holds the output at +15 volts.

Current limiting for the +15 V supply is provided by the internal circuitry of the three-terminal regulator. Diodes CR576 and CR583 protect U570A from transient voltage reversals.

+8 V Regulator

The +8 V Regulator is composed of Q465, Q479, U470A, U470B, and the associated components. The circuit regulates the voltage and limits the supply current.

Initially, as power is applied, the voltage at pin 6 of U470B via R476 is lower than the +8 V reference level applied to pin 5 via divider R465 and R466. The output of U470B is forced HI, reverse biasing diode CR466. With CR466 (and CR465) off, all the current through R565 is supplied as base current to Q465, turning it on. This turns on the pass transistor Q479 at maximum current. This current charges up the various loads on the supply line and the output level moves positive.

As the regulator output rises toward +8 V, this positive-going voltage is applied to the inverting input of U470B through R476. When the output voltage reaches +8 V, the inverting input equals the reference at the noninverting input set by R465 and R466. Then, the output at pin 7 of U470B goes negative, forward biasing diode CR466 and shunting base-drive current away from Q465. This reduces the currents through Q465 and Q479 to levels that maintain a +8 V output. Since base drive source for Q465 is the +15 V supply, via R565, proper relative polarity between the two supplies is assured (preventing component damage in case of a failure on the +15 V supply line).

The over-current limiting circuit is of foldback design and is performed by operational amplifier U470A and its associated components. Under normal current demand conditions, the output of U470A is HI, keeping diode CR465 reverse biased. If the regulator output current exceeds approximately 1.3 A (as it might if a component fails), the voltage drop across R473 (added onto the +8 V output voltage) causes the inverting input of U470A to exceed the +8 V level at the noninverting input, and the output at pin 1 will go LO. This forward biases diode CR465 and reduces the forward bias on Q465 and thereby decreases the bias current to Q479. This in turn reduces the regulator output current through Q479 to decrease the output voltage. As the output voltage drops (applied to U470A pin 3), the output current required to cause limiting also decreases, causing both voltage and current to drop to low values as Q465 becomes biased off.

Pin 2 of U470A is pulled down through R477 to the $-8\ V_A$ supply so that the output of the foldback circuit becomes immediately HI at power-on. This initial HI holds CR465 biased off thereby preventing a false overcurrent sense and subsequent latchup at start-up as the +8 V regulated output seen on pin 3 of U470A rises from zero volts to its normal operating level.

+5 V Regulator

Regulation of the +5 V supply is provided by a circuit similar to that of the +8 V Regulator. As long as the relative polarity between the +8 V supply and the +5 V supply is maintained, base drive to Q870 is supplied through R864. The current through Q870 provides base drive for the series-pass transistor Q879.

When voltage-sense amplifier U870B detects that the +5 V remote-sense voltage has reached +5 V, it begins shunting base-drive current away from Q870 via diode CR866 and holds the output voltage constant.

Current limiting for the +5 V supply is done by U870A and associated components. Under normal current demand conditions, the output of U870A is high and diode CR865 is reverse biased. However, should the current through current-sense resistor R873 reach approximately 3 amperes, the voltage developed across R873 (added to the regulated +5 V output) raises the voltage at pin 2 of U870A (via divider R876 and R875) to a level equal to that at pin 3. This causes the output of U870A to go low, forward biasing CR865. Base drive current is then shunted away from Q870, and the output current in Q879 is reduced. Resistor R874 allows the supply to maintain regulation with the remote-sense line disconnected. Resistors R885 and R886 provide enough initial current to the load to prevent an excessive-current latchup of U470A as the power comes up.

−15 V Regulator

Operation of the −15 V Regulator, composed of U679, U570B and their associated components, is similar to that of the +15 V Regulator already described. The regulator is referenced to −5 V to allow sensing of the negative output level. Zener diode VR870 allows operational amplifier U570B to operate in its active region. Capacitor C873 is a speed-up capacitor that allows the regulator to respond more quickly to current surges and other transients and provides filtering of zener noise produced by VR870.

−8 V Regulator

Operation of the −8 V regulator is nearly identical to that of the +8 V Regulator, except that it is referenced to −5 V to allow sensing of negative voltages. Zener diode VR380 allows operational amplifiers U270A and U270B to operate in their linear regions.

The −8 V Sense input provides for remote sensing of the supply level on the Main board where regulation is the most critical. Since the −8 V level is remotely sensed, the IR drop caused by the impedance in the supply bus lines

going to the main board and a small series resistor in the line (R121 on the Main board) causes the actual output level from the supply regulator to be closer to −8.4 V. (This is the voltage actually required by some of the −8 V load circuits.) Resistor R388 allows the supply to maintain regulation with the remote sense line disconnected. Current limiting of the combined −8 V and −8.3 V supplies occurs at about 3 amperes.

−5 V Regulator

Operation of the −5 V Regulator is similar to that of the +5 V Regulator. Current limiting of the −5 V supply occurs at about 3.1 amperes.

+5 V Inverter Feedback

Operational amplifier U189 and associated components are configured as a frequency-compensated voltage-sensing network. The circuit monitors the +5 V digital power supply line from the rectifiers and provides feedback to the Preregulator Control IC (U233) via optoisolator U155 (both on diagram 22). The feedback is used to trim the +5 V_D level by controlling the Preregulator. The FEEDBACK signal slightly varies the voltage to the Inverter output transformer and holds the output of the 5 V secondary windings at an optimum level. Output levels of the other secondary windings are related by turns ratio to the +5 V_D level and are also held at their optimum levels. This technique minimizes power losses in the series-pass transistors and increases regulator reliability.

Power-Up

The Power-Up circuit, composed of U189A, Q295 and the associated components, provides buffering and level shifting of the LINE UP signal to the System Processor.

Operational amplifier U189A is configured as a comparator referenced to +10 V_{REF}. When adequate power-line input voltage is available, the LINE UP signal will be HI. The output of the comparator will be LO, turning off transistor Q295. This results in a HI PWRUP signal to the System μP, indicating that the power supplies are stable. When adequate power-line voltage is not available, the LINE UP signal from the Preregulator circuit goes LO, the output level of U189A goes HI and turns Q295 on, resulting in a LO PWRUP signal to the System μP. This indicates that the various supply voltages may go out of regulation in about 10 ms.

Capacitor C195 provides a negative-feedback path for high-frequency signals and stabilizes operation of U189A.

DC-OK Sense

The output of the DC-OK Sense circuit is checked by the System Processor after it receives the PWR UP signal to verify that power supply voltages are within tolerance.

By itself, the resistive summing network made up of R794, R795, R797, R686, R688 and R796 would produce a voltage near zero volts if all supplies were within tolerance. This voltage may vary ±0.19 V, depending on slight variations in the individual supply output levels. The current in resistor R396 is, however, added into the summing node and shifts its operating point approximately 0.19 V positive.

The resulting voltage is compared to ground by comparator U395B and to +0.37 V by comparator U395A, establishing the tolerance window. Both open-collector outputs of the comparator are off, and the DCOK signal is HI, as long as the summing-node voltage falls within this window. Should the summing-node voltage exceed either limit, the associated comparator turns on its output transistor and pulls the DCOK signal LO, indicating that at least one of the power supplies is not operating properly.

PERFORMANCE CHECK AND FUNCTIONAL VERIFICATION PROCEDURE

NOTE

Perform the SELF-CAL procedure before doing this procedure. A demonstration procedure of SELF CAL is given in "Operator's Familiarization," Section 2, and a detailed description of the built-in calibration and diagnostics is given in Appendix A of this manual.

INTRODUCTION

Use this procedure to verify proper operation of instrument controls and to check the instrument's performance against the requirements listed in Section 6. This procedure verifies instrument function and may be used to determine need for readjustment (all internal adjustments should be referred to qualified service personnel). These checks may also be used as an acceptance test.

Do not remove this instrument's cabinet to perform this procedure. All checks are made using the operator-accessible front- and rear-panel controls and connectors.

Within the procedure, there are steps that verify proper operation of instrument controls or functions that are not specified as Performance Requirements in Section 6. These steps use the word "VERIFY" when indicating the characteristic for which to test. The functions tested by these steps ARE NOT Performance Requirements and should not be interpreted as such. Steps to check Performance Requirements use the word "CHECK", rather than "VERIFY".

PREPARATION

THIS PROCEDURE ASSUMES THAT OPERATORS ARE SUFFICIENTLY ACQUAINTED WITH INSTRUMENT OPERATION TO SET IT UP AS DIRECTED IN THE PROCEDURE STEPS. Familiarization procedures are found in Sections 1 and 2 of the Operators Manual included with this instrument. Section 5 of that manual is a reference for operation of all front- and rear-panel controls and connectors. Refer to those sections of the Operators Manual if instructions for obtaining the various operation modes of this instrument are needed.

Test equipment items 1 through 24 listed in Table 4-1 are required to perform this procedure (items 20 and 22 through 24 are only needed with instruments having the Video Option). The specific pieces of equipment required to perform the checks within each subsection are listed at the beginning of that subsection. The item numbers in parenthesis next to each piece of equipment refer to the numbered equipment list of Table 4-1. Items 25 through 28 are used for instrument calibration only (see the Adjustment Procedure—Section 5).

Before performing this procedure, ensure that the LINE VOLTAGE SELECTOR switch is set for the ac power source being used (see "Preparation for Use" in Section 2 of this manual). Connect the instrument to be checked and the test equipment to an appropriate power source. Turn the instrument on and ensure that no error message is displayed on the CRT. If an error message is present, have the instrument repaired by a qualified service technician before performing this procedure.

This procedure is divided into subsections (VERTICAL SYSTEM, TRIGGERING SYSTEM, etc.), and further into steps (Verify CH1 and CH2 50 Ω Overload Protection, etc.). This arrangement allows verification of the functionality of the instrument's individual sections, as well as its conformance to individual specifications, without requiring performance of the entire procedure. Any number of

Table 4-1
Test Equipment Required

NOTE

Item numbers 20 and 22 through 24 are needed for checking the 2440 TV Option 05 only.

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
1. Leveled Sine-Wave Generator (Primary)	Frequency: 250 kHz to 250 MHz. Output amplitude: variable from 5 mV to 5 V p-p. Output impedance: 50 Ω. Reference frequency: 50 kHz. Amplitude accuracy: constant within 3% of reference frequency as output frequency changes.	Vertical, horizontal, and triggering checks and adjustments.	TEKTRONIX SG 503 Leveled Sine Wave Generator.[a]
2. Leveled Sine-Wave Generator (Secondary)	Frequency: 245 MHz to 500 MHz. Output amplitude: variable from 500 mV to 4 V p-p. Reference frequency: 6 MHz. Amplitude accuracy (at reference): within 3% of indicated amplitude.	Bandwidth and transient response checks and adjustments.	TEKTRONIX SG 504 Leveled Sine Wave Generator with Leveling Head.[a]
3. Calibration Generator	Standard-amplitude signal levels: 5 mV to 50 V. Accuracy: ±0.25%, ±1 μV. Repetition Rate: 1 kHz. High-amplitude signal levels: 1 V to 60 V. Repetition rate: 1 kHz. Fast-rise signal level: 100 mV to 1 V. Repetition rate: 100 Hz to 100 kHz. Rise time: 1 ns or less. Flatness: ±0.5%.	Signal source for gain.	TEKTRONIX PG 506 Calibration Generator.[a]
4. Time-Mark Generator	Marker outputs: 10 ns to 0.5 s. Marker accuracy: ±0.0002%. Trigger output: 1 ms to 0.1 μs, time-coincident with markers.	Horizontal checks.	TEKTRONIX TG 501 Time Mark Generator.[a]
5. Function Generator	Range: less than 1 Hz to 80 kHz; sinusoidal output; amplitude variable to greater than 10 V p-p open circuit with dc offset adjust.	Low-frequency checks.	TEKTRONIX FG 502 Function Generator.[a]
6. Power Supply	Range: 0 to 20 VDC.	50 Ω Overload verification.	TEKTRONIX PS 503A Power Supply.[a]
7. Digital Voltmeter (DMM)	Range: 0 to 140 V. Dc voltage accuracy: ±0.15%. 4-1/2 digit display.	Sequencer Input/Outputs Verification	TEKTRONIX DM 501A Digital Multimeter.[a]
8. GPIB Controller	Conform to IEEE-488 (1978) standard.	Check GPIB operation.	TEKTRONIX 4041 System Controller.
9. GPIB Cable	Conform to IEEE-488 (1978) standard.	Check GPIB operation.	Tektronix Part Number 012-0630-03.
10. Coaxial Cable (2 required)	Impedance: 50 Ω. Length: 42 in. Connectors: BNC.	Signal interconnection.	Tektronix Part Number 012-0057-01.
11. Precision Coaxial Cable	Impedance: 50 Ω. Length: 36 in. Connectors: BNC.	Used with Calibration Generator.	Tektronix Part Number 012-0482-00.

Table 4-1 (cont)

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
12. Termination	Impedance: 50 Ω. Connectors: BNC.	Signal termination.	Tektronix Part Number 011-0049-01.
13. 10X Attenuator (2 required)	Ratio: 10X. Impedance: 50 Ω. Connectors: BNC.	Vertical and triggering checks.	Tektronix Part Number 011-0059-02.
14. 5X Attenuator	Ratio: 5X. Impedance: 50 Ω. Connectors: BNC.	Vertical and triggering checks.	Tektronix Part Number 011-0060-00.
15. 2X Attenuator	Ratio: 2X. Impedance: 50 Ω. Connectors: BNC.	External triggering checks.	Tektronix Part Number 011-0069-02.
16. 10X Standard Accessory Probe (supplied with instrument)	DC to 250 MHz probe.	Signal input connector.	TEKTRONIX P6136.
17. 1X Probe	DC to 34 MHz probe.	Signal input connector.	TEKTRONIX P6101A.
18. Dual-Input Coupler	Connectors BNC female-to-dual-BNC male.	Signal interconnection.	Tektronix Part Number 067-0525-01.
19. BNC Female-to-Dual Adapter (2 required)	Connectors BNC female-to-dual-banana male.	Signal interconnection.	Tektronix Part Number 103-0090-00.
20. Sine-Wave Oscillator	Frequency: adjustable to 60 Hz. Amplitude: adjustable to 3 V p-p into 75 Ω.	Check TV triggers for back-porch clamp operation.	TEKTRONIX SG 502 Oscillator.[a]
21. Pulse Generator	Period Range: 1 ms to 2 μs. Pulse Range: 0.5 ms to 1 μs. Amplitude variable from −5 to +5 V, independent pulse top and pulse bottom.	Verify and Check Sequencer Input/Outputs. Check TV triggers for sync separation, Option 05 only.	TEKTRONIX PG 502 Pulse Generator.
22. Sync and Linearity Test Generator	Conforms to TV System requirements.	Check TV triggers for back-porch clamp and video modes operation.	TEKTRONIX R147A NTSC Test Signal Generator. TEKTRONIX R148 Insertion Test Signal Generator.
23. Coaxial Cable (2 required)	Impedance: 75 Ω. Length: 42 in. Connectors: BNC.	Signal interconnection.	Tektronix Part Number 012-0074-00.
24. Termination	Impedance: 75 Ω. Connectors: BNC.	Signal termination.	Tektronix Part Number 011-0055-00.
25. Alignment Tool	Length: 1 in. shaft. Bit size: 3/32 in. Low capacitance; insulated.	Adjust variable capacitors and resistors.	Tektronix Part Number 003-0675-00.
26. Normalizer	Input Resistance: 1 MΩ. Input Capacitance: 15 pF.	Check input capacitance.	Tektronix Part Number 067-0537-00.
27. Tunnel-Diode Pulser	Rise time: 125 ps or less.	Adjust transient response.	Tektronix Part Number 067-0681-01.
28. 2.5X Attenuator	Ratio: 2.5X. Impedance: 50 Ω. Connectors: BNC.	Adjust transient response.	Tektronix Part Number 011-0076-01.

[a]Requires a TM 500-Series Power-Module Mainframe.

steps (in any order) can be performed as long as ALL the parts of a step are performed in sequence and in their entirety.

BEFORE PERFORMING THE REMAINDER OF THIS PROCEDURE, DO THE "INITIAL SETUP" AT THE BEGINNING OF THE PROCEDURE STEPS. The Initial Setup is a procedure for setting up and storing a complete front-panel setup that can be recalled. When performing almost any step in this procedure, the first part (part a) requires that this stored front-panel setup be recalled and specifies the changes (if any) to be made to that setup. Make ONLY those changes specified; do not change any other control settings (including vertical and horizontal position settings).

NOTE

This instrument must be powered up for at least 20 minutes before performance requirements can be checked.

"Select" means to press the appropriate front panel button to obtain the stipulated menu on the CRT screen. "Set", when preceded by a menu selection, indicates the stipulated menu function should be turned on or off by pressing the appropriate menu button. The function will appear underlined in the menu when turned on, not underlined when turned off. Control settings not listed do not affect the procedure.

INITIAL SETUP

a. Select PRGM.

Push:		INIT PANEL
Select TRIGGER MODE		
Set:	AUTO	ON
Select VERTICAL MODE		
Set:	CH2	On
Select CH1 COUPLING/INVERT		
Set:	50Ω ON;OFF	ON
Select CH2 COUPLING/INVERT		
Set:	50Ω ON;OFF	ON
Set:	A SEC/DIV	500 μs

b. Select the A/B TRIG button to enable the B Trigger System.

c. Select TRIGGER MODE to display B TRIG MODE menu and set TRIG AFTER ON. Select the A/B TRIG button to return to the A Trigger System.

d. Select STORAGE ACQUIRE and set REPET ON;OFF ON. Repeatedly press the menu button labeled AVG until a "16" appears above the AVG. Repeatedly press the ENVELOPE button until a "16" appears above ENVELOPE. Set NORMAL back on.

e. Select PRGM to display the main SEQUENCER menu. Press SAVE in the main menu to display the SAVE Sequence menu.

f. Use the arrows under ROLL-CHARS to create a label (use FPNL) for the front-panel setup as outlined here in steps a-d:

1. Select the first character for the label. Use the arrow-labeled buttons to select the first letter for the sequence label. Press the ↓ button to step forward in the alphabet and digit (0-9) and the ↑ button to step backwards. Holding down the buttons moves through the character continuously; a single press moves forward or backward one character. (There is a "blank space" character between the digit 9 and letter A.)

2. When the letter for the first character of the label is displayed, push CURSOR <> to move to the next character. Repeat step a to select the letter for the next character of the label.

3. Repeat last step until "FPNL" is spelled out. (Any character can be returned to for editing by continually pushing the cursor button, since it reverses the selection order after the first and sixth character is selected.)

g. Push menu button labeled SAVE when the label is complete.

NOTE

In part h, Trigger Mode is set back to AUTO LEVEL. (AUTO LEVEL was initially turned off to make the front-panel changes in parts a through g faster to set.) Throughout the remainder of this Performance Check procedure, the scope is switched to AUTO

LEVEL when the initial setup is recalled, providing automatic triggering of displays. If preferred, you can switch to AUTO and use INIT @50% and/or the TRIGGER LEVEL control to trigger manually. When AUTO is the required mode for a procedure (such as for checking the Trigger Level Readout accuracy, etc.) AUTO is specified in that procedure.

Occasionally, AUTO LEVEL may fail to find a stable trigger if you connect the triggering signal to the front panel between auto-level cycles; if so, push INIT @50% to obtain the triggered display.

h. Pushing the menu button saves the label for the sequence and displays the message "SETUP CONTROLS, PUSH PRGM TO CONTINUE." Select TRIGGER MODE and set AUTO LEVEL on. *DO NOT CHANGE ANY OTHER FRONT-PANEL SETTINGS AT THIS TIME.* Instead, save the current front-panel setup by doing the following:

1. Push the front-panel button PRGM. This will bring up the action selection menu.

2. Do not select any actions. Push the menu button labeled SAVE SEQ to store the sequence under the label "FPNL".

i. Later in this procedure, when instructed to recall the "Initial Front-Panel Setup", perform the following steps:

1. Push PRGM to display the main SEQUENCER menu.

2. Push RECALL in the main menu to display the menu used for recalling the front-panel Setup.

3. Use the arrow-labeled buttons to move the underline to the label "FPNL".

4. Push RECALL and the front-panel settings will change to those settings that were stored for FPNL.

Remember this four-step procedure for recalling FPNL.

NOTE

The following steps turn the Trigger Point Indicator (a small "T" displayed on waveforms) and the BELL on for use in this procedure. These functions cannot be stored in the front-panel setup, but remain in effect until changed by the operator. Leave these functions turned on for the remainder of this procedure.

j. Press the MENU OFF/EXTENDED FUNCTIONS button twice to display the EXTENDED FUNCTION menu. Press the menu button labeled SYSTEM (menu will change).

k. Press the menu button labeled MISC (menu will change). Set TRIG T ON¦OFF and BELL ON¦OFF to ON for the displayed menu.

l. Press MENU OFF/EXTENDED FUNCTIONS to exit the extended functions.

VERTICAL SYSTEM

NOTE

Before performing the steps in this subsection, perform the INITIAL FRONT PANEL CONTROL SETUP at the beginning of this procedure.

EQUIPMENT REQUIRED (see Table 4-1)

Leveled Sine-Wave Generator (Item 1)
Calibration Generator (Item 3)
Power Supply (Item 6)
Coaxial Cable (Item 10)
Precision Coaxial Cable (Item 11)
10X Attenuator (Item 13)
5X Attenuator (Item 14)
2X Attenuator (Item 15)
10X Probe (Item 16)
1X Probe (Item 17)
Dual-Input Coupler (Item 18)

1. Verify CH 1 and CH 2 50 Ω OVERLOAD Protection.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select TRIGGER MODE		
Set:	AUTO	ON
Set:	CH 1 VOLTS/DIV	1V
	CH 2 VOLTS/DIV	1V
Select VERTICAL MODE		
Set:	CH 2	Off
Select CH 1 COUPLING/INVERT		
Set:	50Ω ON¦OFF	OFF
Select CH 2 COUPLING/INVERT		
Set:	50Ω ON¦OFF	OFF

b. Connect the Power Supply (Power Supply should be turned off) to the CH 1 OR X input connector via a BNC female-to-dual banana adapter and a 50-Ω BNC cable.

c. Using the CH 1 VERTICAL POSITION control, align the trace to the bottom graticule line.

d. Turn on the Power Supply.

e. Adjust the Power Supply output level until the CH 1 trace rises to 1 division above the center graticule line (5 V).

f. Select CH 1 COUPLING/INVERT and set 50Ω ON¦OFF to ON.

g. VERIFY—For a period of 1 minute, the readout display does not indicate any overload condition (50Ω OVERLOAD).

h. Set 50Ω ON¦OFF to OFF and the CH 1 VOLTS/DIV to 5 V.

CAUTION

To prevent damage to the input circuitry when in 50-Ω DC coupling mode, the 20V Power Supply should be turned off immediately if automatic OVERLOAD switching does not occur within 15 seconds after applying the power source and setting the 50-Ω coupling on in part j.

i. Increase the Power Supply output level until the CH 1 trace rises to the center graticule line (+20 V).

j. Set 50Ω ON¦OFF to ON.

k. VERIFY—Approximately 10 seconds (no longer than 15 seconds) after CH 1 50Ω ON¦OFF is set to ON, the readout display indicates "50Ω OVERLOAD" and the CH 1 COUPLING switches to GND.

l. Turn the Power Supply off.

m. Disconnect the Power Supply.

n. Clear the 50Ω OVERLOAD condition by setting CH 1 COUPLING to DC.

o. VERIFY—The readout display no longer indicates "50Ω OVERLOAD" and the CH 1 COUPLING/INVERT menu indicates DC on.

p. Select VERTICAL MODE and set CH 1 off and CH 2 on.

q. Repeat b through n using CH 2 control settings and input to verify 50Ω OVERLOAD protection for CH 2.

2. Check CH 1 and CH 2 AC/DC/GND COUPLING/INVERT Modes.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set:	CH 1 VOLTS/DIV	200mv
	CH 2 VOLTS/DIV	200mV
Select VERTICAL MODE		
Set:	CH 2	Off
Select CH 2 COUPLING/INVERT		
Set:	50Ω ON¦OFF	OFF
	GND	On
Select CH 1 COUPLING/INVERT		
Set:	50Ω ON¦OFF	OFF
	GND	On
Set:	A SEC/DIV	5ms

b. Connect the CALIBRATOR output signal to the CH 1 OR X input connector using a 1x probe.

c. Set the CH 1 COUPLING/INVERT menu to DC on (a GND symbol disappears next to the CH 1 scale factor readout).

d. CHECK—Display for a square wave which steps positive (upwards) approximately 2 divisions from the center horizontal graticule line.

e. Set CH 1 COUPLING to AC (a sine wave symbol appears next to the CH 1 scale factor readout in upper left-hand corner of CRT).

f. CHECK—Display for a tilted square wave of approximately 2 divisions (average) amplitude centered vertically around the center horizontal graticule line.

g. Set 50Ω ON¦OFF to ON (the sine wave symbol is replaced by an ohm symbol next to the CH 1 scale factor readout).

h. CHECK—Display for a square wave which steps positive (upwards) approximately 0.5 division from the center horizontal graticule line. VERIFY—That CH 1 COUPLING automatically switched from AC on to DC on.

i. Set INVERT ON¦OFF to ON (an inverted arrow appears left of the CH 1 scale factor readout.

j. CHECK—Displayed square wave now steps downwards from the center horizontal graticule line and is approximately 0.5 division in amplitude.

NOTE

Amplitudes are less than 1 division (200 mV) for checks h and j since the X1 probe's resistance is significant when compared to the 50-Ω inputs of the scope.

k. Select VERTICAL MODE and set CH 2 on and CH 1 off. Select CH 2 COUPLING/INVERT to display that menu.

l. Move the probe from the CH 1 input connector to the CH 2 input connector.

m. Repeat parts c through j using the CH 2 input and controls.

n. Disconnect the test setup.

3. Check CH 1 and CH 2 VOLTS/DIV Display and Readout Accuracies. Check the A and B TRIGGER LEVEL Readout Accuracies.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Select CH 1 COUPLING/INVERT		
Set:	50Ω ON¦OFF	OFF
Select CH 2 COUPLING/INVERT		
Set:	50Ω ON¦OFF	OFF
Select BANDWIDTH		
Set:	20 MHz	On
Select TRIGGER MODE		
Set:	AUTO	On

b. Connect the Calibration Generator's STD AMPLITUDE output to the CH 1 OR X input connector via a 50-Ω cable. Do not use a termination.

c. CHECK—CH 1 and CH 2 VOLTS/DIV and TRIGGER LEVEL readout accuracies as follows:

1. Set VOLTS/DIV control to the first position listed in Table 4-2.

2. Set the Calibration Generator STD AMPLITUDE output level to the corresponding Standard Amplitude Input Level in Table 4-2. Use the TRIGGER LEVEL control as necessary to obtain a stable display.

NOTE

To properly verify TRIGGER LEVEL readout accuracy the Calibration Generator's output must have rising and falling transition times (10% to 90%) > 20 nanoseconds. No overshoot should appear on the waveform.

3. Verify that the generator output meets the requirements noted above.

4. Use the VERTICAL POSITION control to set the bottom of the signal 3 divisions below graticule center.

5. Select CURSOR FUNCTION and set VOLTS on.

6. Using the CURSOR/DELAY control, align the selected cursor (segmented) with the bottom of the displayed waveform.

7. PUSH the CURSOR SELECT button to select the other cursor (it will change from solid to segmented).

8. Use the CURSOR/DELAY control to align this cursor to the top of the waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in subpart 6.

9. CHECK—That the voltage reading displayed by the cursor readout is within the limits given in Table 4-2 under the Readout Accuracy Limits-NORMAL MODE column.

10. Select STORAGE ACQUIRE and set ENVELOPE on.

11. Using the CURSOR/DELAY control, readjust the cursors as necessary to align them to the top or bottom (discount noise) of the waveform. Press CURSOR SELECT as needed to toggle between the two cursors.

12. CHECK—That the voltage reading displayed is within the limits given in Table 4-2 under the Readout Accuracy—ENVELOPE MODE column.

13. Set the ACQUIRE menu back to NORMAL on.

14. Set the TRIGGER LEVEL control at the most positive voltage that produces a barely triggered, jittering display for the positive (+) setting for the slope switch.

15. CHECK—The A Trigger Level readings (upper-right corner of display) are within the limits listed in the (+) Peak column under DC Coupling in Table 4-2.

16. Set the TRIGGER LEVEL control at the most negative voltage that produces a barely triggered, jittering display for negative (—) setting for the slope switch.

17. CHECK—The A Trigger Level readings are within the limits listed in the (—) Peak column under DC Coupling in Table 4-2.

18. Set the TRIGGER LEVEL control for a stable display.

19. Press the A/B TRIG button to set the B Trigger System on.

20. Set HORIZ MODE to B.

21. Set the TRIGGER LEVEL control at the most positive voltage that produces a barely triggered, jittering display for the positive (+) setting for the slope switch.

22. CHECK—That the B Trigger Level readings (upper-right corner of display) are within the limits listed in the (+) Peak column under DC Coupling in Table 4-2.

23. Set the TRIGGER LEVEL control at the most negative voltage that produces a barely triggered, jittering display for negative (—) setting for the slope switch.

24. CHECK—That the B Trigger Level readings are within the limits listed in the (—) Peak column under DC Coupling in Table 4-2.

25. Set the HORIZ MODE to A.

26. Press the A/B TRIG button to set the A Trigger System on.

27. Set the VOLTS/DIV control to the next position listed in Table 4-2.

28. Set the Calibration Generator STD AMPLITUDE output level to the corresponding Standard Amplitude Input Level in Table 4-2.

29. Use the VERTICAL POSITION control to set the bottom of the signal 3 divisions below graticule center.

30. Repeat subparts 6 through 29 for each VOLTS/DIV setting listed in Table 4-2. Skip subparts 26 through 29 when checking the last VOLTS/DIV setting in the table.

31. Press A/B TRIG to set the B Trigger System on. Select TRIGGER CPLG and set REJECT NOISE on.

32. Press A/B TRIG to set the A Trigger System on (the A TRIG CPLG menu will be displayed). Set REJECT NOISE on.

33. CH 1 VOLTS/DIV control to 50 mV.

34. Set the Calibration Generator's STD AMPLITUDE output level to .2 V.

35. Repeat subparts 14 through 24, using 147 mV to 253 mV as the limits to check against in subparts 15 and 22 and +47 mV to —47 mV as the limits for subparts 17 and 24.

36. Set the B COUPLING mode back to DC on (B TRIGGER CPLG menu is still displayed from subpart 24).

37. Press the A/B TRIG button to set the A Trigger System on (the A COUPLING menu will be displayed). Set A COUPLING to DC on.

38. Set HORIZONTAL MODE to A.

39. Set the CH 1 VOLTS/DIV control to 1 V and the Calibration Generator's output level to 5 V.

40. Select CH 1 VARIABLE and press and hold down the menu button labeled "↓" until the displayed waveform no longer decreases in amplitude.

41. CHECK—That the amplitude of the displayed waveform is two divisions or less. VERIFY—That a ">" symbol appears immediately left of the CH 1 scale factor readout.

42. VERIFY—That the amplitude of the displayed waveform increases when the menu button labeled "↑" is pushed.

43. Press CAL. VERIFY—That the waveform has returned to its original amplitude and that the ">" symbol is no longer displayed.

44. Select CH 1 COUPLING/INVERT and set INVERT ON¦OFF to ON.

45. Using the VERTICAL POSITION control, set the bottom of the waveform 3 divisions below graticule center.

46. Repeat subparts 6 through 9 to check INVERT accuracy.

47. Return INVERT ON¦OFF to OFF.

48. Select VERTICAL MODE and set CH 2 on and CH 1 off. Move the cable to CH 2 OR Y.

49. Repeat subparts 1 through 48 (skipping 5) to check the functions and accuracies for CH 2.

50. Select TRIGGER MODE and set AUTO LEVEL on.

Table 4-2

Accuracy Limits CH 1 and CH 2 CURSOR VOLTS Readout and A and B TRIGGER LEVEL Readouts

VOLTS/DIV Control	Standard Ampl Out	CURSOR VOLTS Readout Accuracy		TRIGGER LEVEL Readout Limits—DC Coupling	
		NORMAL (2% + 0.04 div)	ENVELOPE (3% + 0.04 div)	+ Peak	− Peak
2 mV	10 mV	9.72 mV-10.28 mV	9.62 mV-10.38 mV	8.5 mV-11.5 mV	±1.2 mV
5 mV	20 mV	19.40 mV-20.60 mV	19.20 mV-20.80 mV	17.2 mV-22.8 mV	±2.2 mV
10 mV	50 mV	48.60 mV-51.40 mV	48.10 mV-51.90 mV	44.4 mV-55.6 mV	±4.0 mV
20 mV	0.1 V	97.20 mV-102.80 mV	96.20 mV-103.80 mV	89.6 mV-110.4 mV	±7.2 mV
50 mV	0.2 V	194.00 mV-206.00 mV	192.00 mV-208.00 mV	178.0 mV-222.0 mV	±16.0 mV
100 mV	0.5 V	486.00 mV-514.00 mV	481.00 mV-519.00 mV	448.0 mV-552.0 mV	±36.0 mV
200 mV	1 V	972.00 mV-1.03 V	962.00 mV-1.04 V	896.0 mV-1.1 V	±72.0 mV
500 mV	2 V	1.94 V-2.06 V	1.92 V-2.08 V	1.8 V-2.2 V	±160.0 mV
1 V	5 V	4.86 V-5.14 V	4.81 V-5.19 V	4.5 V-5.5 V	±360.0 mV
2 V	10 V	9.72 V-10.28 V	9.62 V-10.38 V	9.0 V-11.0 V	±710.0 mV
5 V	20 V	19.40 V-20.60 V	19.20 V-20.80 V	17.8 V-22.2 V	±1.6 V

51. Remove the cable from CH 2 OR Y input and connect the 5-V standard amplitude signal to CH 1 OR X and CH 2 OR Y through a Dual-Input Coupler.

52. Using the CH 2 VERTICAL POSITION control, set the bottom of the CH 2 waveform to graticule center.

53. Select VERTICAL MODE and set CH 1 on. Use the CH 1 VERTICAL POSITION to superimpose the CH 1 waveform exactly over the CH 2 waveform.

54. Set CH 1 and CH 2 VOLT/DIV controls to 5 V. Set CH 1 and CH 2 off and ADD on.

55. Align the cursors to the top and bottom of the displayed waveform as in subparts 6 and 7.

56. VERIFY—That the readout indicates about 10V.

57. Set CH 1 and CH 2 VOLTS/DIV to 2 V and set MULT on (ADD will be turned off).

58. Align the cursors to the top and bottom of the displayed waveform as in subparts 6 to 7.

59. VERIFY:—That the readout indicates about 25 V^2.

d. Set MULT off and CH 1 on. Set CH 1 to 1 V.

e. Precisely align one voltage cursor to the graticule line 3 divisions above graticule center and the other cursor to the line 3 divisions below graticule center.

f. CHECK—That the voltage reading displayed is within 1% of 6.00 Volts (5.94 to 6.06).

g. Disconnect the test setup.

4. Check LF Linearity.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Select CH 1 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Select CH 2 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF

b. Connect the Calibration Generator's STD AMPLITUDE output to the CH 1 OR X input connector via a 50-Ω cable. Do not use a termination.

c. Set the Calibration Generator's STD AMPLITUDE output level to .2 V.

d. Use the CH 1 POSITION control to center the waveform vertically around the center horizontal graticule line.

e. Use the generator's VARIABLE control to adjust the waveform for exactly 2 vertical divisions on screen (discount trace width).

f. Use the CH 1 POSITION control to align the top of the waveform to the top horizontal graticule line.

g. CHECK—That the amplitude of the displayed waveform is between 1.88 and 2.12 divisions.

h. Use the CH 1 POSITION control to align the bottom of the waveform to the bottom horizontal graticule line.

i. CHECK—That the amplitude of the displayed waveform is between 1.88 and 2.12 divisions.

j. Select STORAGE ACQUIRE and set ENVELOPE on.

k. Repeat parts d through i to check the LF Linearity for the ENVELOPE mode. Discount the noise and the

envelope "fill" when performing parts g and i and use 1.84 and 2.16 divisions as limits for those parts.

l. Set the STORAGE ACQUIRE mode back to NORMAL on.

m. Move the cable from the CH 1 OR X input to the CH 2 OR Y input.

n. Select VERTICAL MODE and set CH 2 on and CH 1 off.

o. Repeat parts d through k to check CH 2 using CH 2 control settings and menus.

p. Disconnect the test setup.

5. Check CH 1 and CH 2 Position Range.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set:	CH 1 VOLTS/DIV	20mV
	CH 2 VOLT/DIV	20mV
	A SEC/DIV	10μs
Select VERTICAL MODE		
Set:	CH 2	Off

b. Connect a 50-kHz reference frequency signal from the Leveled Sine-wave Generator to the CH 1 OR X input connector via a 50-Ω BNC cable and a 5X attenuator.

c. Adjust the generator's output level for a 4-division display on screen.

d. Remove the 5X attenuator and connect the cable directly to the CH 1 input.

e. Rotate the CH 1 POSITION control full clockwise and hold until the waveform no longer moves up screen.

f. CHECK—That the bottom of the waveform is within +0.4 to −0.7 division of the center horizontal graticule line.

g. Rotate the CH 1 POSITION control full counterclockwise and hold until the waveform no longer moves down screen.

h. CHECK—That the top of the waveform is within +0.7 to −0.4 division of the center horizontal graticule line.

i. Reinstall the 5X attenuator and move the cable to the CH 2 OR Y input.

j. Select VERTICAL MODE and set CH 2 on and CH 1 off.

k. Repeat parts c through h to check CH 2's position range, using the CH 2 input connector and controls.

6. Check CH 1 and CH 2 Bandwidth and Bandwidth Limit (20 MHz and 100 MHz).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see Step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set:	CH 1 VOLTS/DIV	2mV
	A SEC/DIV	100ns
	CH 2	Off

b. Connect the output of the secondary Leveled Sine-wave Generator (item 2) to the CH 1 input connector via the leveling head included with the generator and any combination of the 10X, 5X, and 2X attenuators that reduces the signal amplitude to the level called for in part c.

c. Set the generator output level for a 6-division display at the 6-MHz reference frequency, then change the output frequency to 300 MHz.

d. Set A SEC/DIV to 2 ns.

e. CHECK—The display amplitude is 4.2 divisions or greater.

f. Return the A SEC/DIV to 100 ns and set the CH 1 VOLT/DIV control to the next higher setting.

g. Repeat parts c through f for all CH 1 VOLTS/DIV settings through 500 mV, removing and/or adding attenuators as necessary to allow adjusting the generator output level to 6 divisions.

h. Select VERTICAL MODE and set CH 2 on and CH 1 off.

i. Set CH 2 VOLTS/DIV to 2 mV and A SEC/DIV to 100 ns.

j. Repeat parts b through g to check CH 2 bandwidth, substituting CH 2 controls and input connector.

k. Set the A SEC/DIV to 10 μs.

l. Disconnect the secondary generator.

m. Connect the output of the primary Leveled Sine-wave Generator (item 1) to the CH 2 input connector via a precision 50- cable and any combination of the 10X, 5X, and 2X attenuators that reduces the signal amplitude to the level called for in part n.

n. Set the primary Leveled Sine-wave Generator to a 50-kHz reference frequency and, changing attenuators as necessary, adjust the output level for a 6-division display.

o. Select VERTICAL BANDWIDTH and set to 20 MHz. Set the A SEC/DIV to 20 ns.

p. Increase the generator's output frequency until the display amplitude is 4.2 divisions.

q. CHECK—That the generator's output frequency is from 13 MHz to 24 MHz.

r. Set VERTICAL BANDWIDTH to 100 MHz and the A SEC/DIV to 5 ns.

s. Increase the generator's output frequency until the display amplitude is 4.2 divisions.

t. CHECK—That the generator's output frequency is from 80 MHz to 120 MHz.

u. Set VERTICAL BANDWIDTH to FULL and A SEC/DIV to 10 μs. Select VERTICAL MODE and set CH 1 on and CH 2 off.

v. Repeat parts m through t to check CH 1 20 MHz and 100 MHz bandwidth limit, substituting CH 1 controls and input connector.

w. Disconnect the test setup.

7. Check Common Mode Rejection Ratio (CMRR).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set:	A SEC/DIV	10μs
Select VERTICAL MODE		
Set:	CH2	Off
	ADD	On
Select CH1 COUPLING/INVERT		
Set:	INVERT ON!OFF	ON
Select TRIGGER SOURCE		
Set:	CHAN1!2	1
Select CURSOR FUNCTION		
Set:	VOLTS	On
Menu displayed: ATTACH CURSORS TO:		
Set:	ADD	On
Select STORAGE ACQUIRE		
Set:	AVG	On

NOTE

When the Initial Front Panel Setup is recalled in part a, the CH 1 and CH 2 traces will be centered vertically. DO NOT adjust the CH 1 or CH 2 POSITION controls during the remainder of this CMRR check to avoid exceeding the dynamic range of the CH 1 and/or CH 2 Vertical systems. If the controls are accidently adjusted, go back to part a and repeat this check.

b. Connect a 50-kHz reference frequency signal from the Leveled Sine-wave Generator to the CH 1 OR X and CH 2 OR Y input connectors via a 50-Ω BNC cable and a Dual-Input Coupler.

c. Set the generator output level for a 5-division display of the reference signal on CH 1.

d. Set the CH 1 and CH 2 VOLT/DIV controls to 50 mV.

e. Select VERTICAL MODE and set CH 1 off.

f. Select CH 2 VARIABLE and, using the menu buttons under the arrow symbols, adjust for minimum ADD display amplitude.

g. Set the A SEC/DIV to 20 ns.

h. Set the generator's output frequency to 50 MHz.

i. Using the CURSOR/DELAY control, align the movable cursor (segmented) to the bottom of the ADD waveform.

j. Press CURSOR/SELECT to enable the alternate cursor.

k. Use the CURSOR/DELAY control to align this cursor to the top of the ADD waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in part i.

l. CHECK—That the cursor readout (upper right corner of display) indicates 50.0 mV or less.

m. Set the generator's output frequency back to 50 kHz.

n. Set the VARIABLE menu back to CAL and return the A TIME/DIV control to 10 μs.

o. Select CH 1 COUPLING/INVERT and set INVERT ON\|OFF to OFF.

p. Select CH 2 COUPLING/INVERT and set INVERT ON\|OFF to ON.

q. Repeat parts f through l to check CMRR with CH 2 inverted. Be sure to use the CH 2 VARIABLE for part f (cursor readout will be in DIV instead of V units if CH 1 VARIABLE is used).

r. Remove the test setup.

8. Check Channel Isolation.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see Step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set:	A SEC/DIV	5 ns
Select CURSOR FUNCTION		
Set:	VOLT	On

(The ATTACH CURSOR menu will be displayed).

NOTE

When the Initial Front Panel Setup is recalled in part a, the CH 1 and CH 2 traces will be centered vertically. DO NOT adjust the CH 1 or CH 2 POSITION controls during the remainder of this Channel Isolation check to avoid exceeding the dynamic range of the CH 1 and/or CH 2 Vertical systems. If the controls are accidently adjusted, go back to part a and repeat this check.

b. Connect the Leveled Sine-wave Generator to the CH 1 OR X input connector via a precision 50-Ω BNC cable.

c. Set the generator frequency to 100 MHz and adjust the output level for a 5-division display.

d. Set the CH 1 and CH 2 VOLTS/DIV controls to 50 mV.

e. Using the CURSOR/DELAY control, align the movable cursor (segmented) to the bottom of the CH 2 waveform.

f. Press CURSOR/SELECT to enable the alternate cursor.

g. Use the CURSOR/DELAY control to align this cursor to the top of the CH 2 waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in part e.

h. CHECK—That the cursor readout (upper right corner of display) indicates 5.00 mV or less.

i. Move the cable to CH 2 input and change CH 2 VOLT/DIV control to 100 mV.

j. Select Trigger Source and set CH 2 on.

k. Set the generator for a 5 divisions in CH 2. Return the CH 2 VOLT/DIV control to 50 mV.

l. Perform parts e-h checking the CH 1 waveform instead of CH 2's to check channel isolation from CH 2 to CH 1.

m. Set both VOLT/DIV controls to 100 mV, the SEC/DIV control to 2 ns, and the Trigger Source back to CH 1.

n. Connect the secondary generator (item 2) to the CH 1 input through the leveling head included with the generator.

o. Set the generator frequency to 300 MHz and adjust the output level for a 5-division display.

p. Repeat parts d-l, using 10.00 mV as the limit for part h, to check 300 MHz channel isolation.

q. Disconnect the test setup.

9. Check the CH 2 Output Voltage Accuracy and Bandwidth.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set:	CH 1 VOLTS/DIV	20mV
Select CH 2 COUPLING/INVERT		
Set:	50-Ω ON¦OFF	OFF
Select TRIGGER SOURCE		
Set:	CHAN1¦2	2
Select CURSOR FUNCTION		
Set:	VOLTS	On
Menu displayed: ATTACH CURSORS TO		
Set:	CH 1	On

b. Connect the Calibration Generator's STD AMPLITUDE output to the CH 2 OR Y input connector via a 50-Ω cable. Do not use a termination.

c. Set the Calibration Generator STD AMPLITUDE output level to .5 V.

d. Use the CH 2 VERTICAL POSITION control to align the bottom of the displayed waveform to the graticule line three divisions below graticule center.

e. Use the generator's VARIABLE AMPLITUDE control to adjust the CH 2 display for precisely 5 divisions amplitude.

f. Connect the CH 2 OUT connector (on the rear panel) to the CH 1 OR X input connector via a 50-Ω BNC cable. Do not use a terminator.

g. Select VERTICAL MODE and set CH 2 off.

h. Use the CH 1 VERTICAL POSITION control to align the bottom of the displayed waveform to the graticule line three divisions below graticule center.

i. Using the CURSOR/DELAY control, align the movable cursor (segmented) to the bottom of the CH 1 waveform.

j. Press CURSOR/SELECT to enable the alternate cursor.

k. Use the CURSOR/DELAY control to align this cursor to the top of the CH 1 waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in part i.

l. CHECK—That the cursor readout (upper right corner of display) indicates 45.00-55.00 mV.

m. Select CH 1 COUPLING/INVERT and set 50 Ω ON¦OFF to OFF.

n. Align the cursors to the displayed waveform as in parts i and k.

o. CHECK—That the cursor readout indicates 90.00-110.00 mV. Set 50Ω ON!OFF back to ON.

p. Disconnect the 50-Ω cable from the Calibration Generator's output and connect it to the output of a Leveled Sine-wave Generator.

q. Select CH 2 COUPLING/INVERT and set 50-Ω ON!OFF to ON.

r. Set the A SEC/DIV control to 200 ns.

s. Set the generator output level for a 6-division display at the 3-MHz reference frequency, then change the output frequency to 50 MHz. Adjust the CH 1 VERTICAL POSITION control as required to view the display.

t. Set the A SEC/DIV control to 5 ns.

u. CHECK—The display amplitude is 4.2 divisions or greater.

v. Disconnect the 50-Ω cable from the CH 2 input.

w. Select CH 1 COUPLING/INVERT and set GND on. Set the A SEC/DIV control to 500 μs.

x. Use the CH 1 VERTICAL POSITION control to align the grounded trace to the center horizontal graticule line.

y. Set the CH 1 VOLTS/DIV to 5 mV and the CH 1 COUPLING to DC.

z. VERIFY—That the trace is within ±2 divisions of the center graticule line.

aa. Disconnect the test setup.

10. Check Display Versus Graticule Centering and Dot Versus Vector Display Offset. Check VECTOR Response for NORMAL and ENVELOPE Acquisition modes.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select VERTICAL MODE		
Set:	CH 2	Off
Select CH 1 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF

b. Press the front-panel button labeled SELECT, and set VECTORS ON!OFF to OFF for the menu displayed.

c. CHECK—That the CH 1 trace is no more than 0.1 division above or below the center horizontal graticule line.

d. Select CURSOR FUNCTION and set TIME on. Note that one cursor is displayed 4 divisions left, one 4 divisions right of the center graticule line. Do NOT adjust the placement of the time cursors displayed.

e. CHECK—That each cursor is located within ±0.1 division of the intersection of the center horizontal graticule line and the vertical graticule line to which it is aligned.

f. Press the menu button labeled TIME to turn off the cursors.

g. Connect the STD AMPL OUTPUT of a Calibration Generator to the CH 1 OR X input connector via a 50-Ω BNC cable.

h. Set the AMPLITUDE control of the generator for a .2 V setting.

i. Select STORAGE ACQUIRE and set AVG on.

j. Press the front-panel button labeled SELECT.

k. Toggle the VECTORS ON!OFF button for the displayed menu, between the ON!OFF settings while making the check in the following part.

l. CHECK—That the display shifts no more than ±0.05 division while performing part k.

m. Disconnect the Calibration Generator from CH 1 connector.

n. Select PRGM and press the menu button labeled INIT PANEL.

o. Select TRIGGER MODE and set AUTO on.

p. Select STORAGE ACQUIRE and set ENVELOPE on. Repeatedly press the ENVELOPE menu button down until CONT (Continuous) appears above the label.

q. Use the CH1 VERTICAL POSITION control to move the displayed trace up 3 divisions and down 3 divisions to create a 6-division "filled" envelope on screen.

r. Press the SELECT button (next to the INTENSITY control).

s. CHECK—For no more than a 0.06-division change in amplitude between the "filled" envelope and the non-filled envelope as VECTORS ON!OFF is switched between the ON AND OFF settings for the displayed menu.

TRIGGERING SYSTEMS

NOTE

The CH 1 and CH 2 Trigger Level Readout Accuracies are checked in the Vertical Systems subsection.

NOTE

In this procedure, a "stable trigger" refers to a consistent trigger; that is, one that results in a uniform, regular display triggered on the selected slope (±). A stably-triggered display should NOT have the trigger point switch between opposite slopes on the waveform, nor should it "roll" across the screen, as successive acquisitions occur. At TIME/DIV settings of 2 ms/DIV and faster, the TRIG'D LED is constantly lit if display is stably triggered (note that, for Tables 4-3 and 4-4, the LED will flash for the 10 ms/DIV checks).

EQUIPMENT REQUIRED (see Table 4-1)

- Primary Leveled Sine-Wave Generator (Item 1)
- Secondary Leveled Sine-Wave Generator (Item 2)
- Time-Mark Generator (Item 4)
- Function Generator (Item 5)
- Coaxial Cable (Item 10)
- Precision Coaxial Cable (Item 11)
- Termination (Item 12)
- 5X Attenuator (Item 14)
- 10X Probe (Item 17)
- Dual-Input Coupler (Item 18)

1. Check A and B Internal Source Trigger Sensitivity.

NOTE

This step checks the CH 1 trigger source for all trigger coupling settings for both A and B Horizontal Modes. The other sources are checked for DC coupling only. Normally, checking all coupling modes for one trigger source is adequate since all the sources share common coupling circuitry; other sources need only be checked in the DC trigger coupling setting to verify their signal paths. However, if a source's trigger sensitivity is very near the limits specified in Table 4-3, this procedure will specify additional checks for the other trigger coupling settings.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE		
Set:	CH 2	Off
Select CH 1 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Select CH 2 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Select TRIGGER MODE		
Set:	AUTO	ON

b. Connect the sine-wave output of the appropriate generator through a 50-Ω cable and a 50-Ω terminator to the CH 1 input connector. Use the Function Generator (item 5) for Test Frequencies below 50 MHz, the Primary Leveled Sine-wave Generator (item 1) for the 50 MHz Test Frequency; and the Secondary Leveled Sine-wave Generator (item 2) for the 300 MHz Test Frequency.

c. Adjust the generator's output frequency to the first Test Frequency setting specified in Table 4-3.

d. Set the SEC/DIV control to the setting used with the Test Frequency.

e. Set the output amplitude of the specified Test Frequency to the level given in Table 4-3 for the A Trigger System with DC Trigger Coupling.

NOTE

When amplitudes of less than 1 division are required, adjust the generator for 10X the specified amplitude with the CH 1 VOLT/DIV set to 100 mV and change the setting to 1 V before making the checks. For amplitudes ≥ to 1 division, simply adjust for the required amplitude with the VOLT/DIV set to 100 mV.

Table 4-3
Minimum Display Level for CH 1 or CH 2 Triggering (in divisions)

Trigger System	Test Frequency	SEC/DIV Setting	TRIGGER COUPLING				
			DC	AC	NOISE REJ	HF REJ	LF REJ
A	60 Hz	10 ms	0.35	0.35	[a]	[a]	(0.35)[b]
B	60 Hz	10 ms	0.70	0.70	[a]	[a]	(0.70)[b]
A	30 kHz	20 μs	0.35	0.35	[a]	0.5	[a]
B	30 kHz	20 μs	0.70	0.70	[a]	1.0	[a]
A	80 kHz	10 μs	0.35	0.35	[a]	[a]	0.5
B	80 kHz	10 μs	0.70	0.70	[a]	[a]	1.0
A	50 MHz	20 ns	0.35	0.35	1.2	(1.2)[b]	0.5
B	50 MHz	20 ns	0.70	0.70	2.4	(2.4)[b]	1.0
A	300 MHz	2 ns	1.0	1.0	3.0	(3.0)[b]	1.0
B	300 MHz	2 ns	2.0	2.0	6.0	(6.0)[b]	2.0
ADD Vertical Mode							
A	300 MHz	2 ns	1.5	1.5	4.5	[a]	1.5
B	300 MHz	2 ns	3.0	3.0	9.0	[a]	3.0

[a]Not necessary to check.

[b]Not triggered at the specified amplitude.

f. Select TRIGGER CPLG to display the A COUPLING menu.

NOTE

When checking for triggers in parts g and h, use the TRIGGER LEVEL control to trigger (or to attempt to trigger) on the waveform.

g. CHECK—For a stable, triggered display on both + and – slopes for all TRIGGER COUPLING settings that are specified at the present Test Frequency.

h. CHECK—For no stable trigger (display free-runs) for any TRIGGER COUPLING setting specifying footnote b—"Not Triggered at specified amplitude."

i. Change the generator output amplitude as necessary and repeat parts g through h for any Trigger Coupling setting specifying a different Minimum Display Level for triggering other than the initial setting for that row. (For example, NOISE, HF, and LF settings usually—but not always—require different amplitudes than the initial setting.)

j. Set the generator's output to the next Test Frequency in Table 4-3.

k. Repeat parts d through j (skip part f) to check A Triggers for each test frequency setting in Table 4-3. Change generators (as specified in part b) as needed to obtain the test frequency required. Return the TRIGGER COUPLING menu to DC when completed.

l. Select VERTICAL MODE and set CH 1 off and CH 2 on.

m. Repeat parts b through k to check CH 2 triggers, using CH 2 control settings and input connector. Skip parts f, h and i and check only for DC trigger coupling in part g if the DC trigger sensitivity is NOT near the specified limits; otherwise, check as for CH 1.

n. Select VERTICAL MODE and set ADD on and CH 2 off.

o. Repeat parts b through k to check ADD triggers, using CH 2 control settings and input connector. Skip parts h and i and check only for DC trigger coupling in part g if the DC trigger sensitivity is NOT near the specified limits; otherwise, check as for CH 1.

p. Select VERTICAL MODE and set ADD off and CH 1 on.

q. Set TRIGGER CPLG back to DC and set the HORIZONTAL MODE to B.

r. Press A/B TRIG to select the B Trigger System (the B COUPLING menu will be displayed).

s. Repeat part b through o to check B triggers, using the TRIGGER LEVEL control to trigger the display. Use the generator amplitude settings specified in the Trigger System-B rows of Table 4-3.

NOTE

When checking 50-MHz and 300-MHz Triggers for the B TRIGGER SYSTEM, the REPET mode acquisitions can require a long time to complete. When setting the B SEC/DIV control for those TEST FREQUENCIES, set the HORIZONTAL MODE to A and set the A SEC/DIV control to the SEC/DIV setting specified in the table. This adjustment will set BOTH A and B Acquisition Systems to the specified SEC/DIV setting and reduce the time required to complete the B REPET acquisition sequence. Set the HORIZONTAL MODE back to B.

t. Disconnect the test setup.

2. Check Trigger Sensitivity for A and B External Sources.

NOTE

This step checks the trigger sensitivity of the external sources for the DC trigger coupling setting only. Normally, checking all coupling modes for one trigger source (checked in step 1 of this subsection) is adequate since all the sources share common coupling circuitry; other sources need only be checked in the DC trigger coupling setting to verify their signal paths. However, if a source's trigger sensitivity is very near the limits specified in Table 4-4, this procedure will specify additional checks for the other trigger coupling settings.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE		
Set:	CH 2	Off
Select CH 1 COUPLING/INVERT		
Set:	50Ω ON¦OFF	OFF
Select CH 2 COUPLING/INVERT		
Set:	50Ω ON¦OFF	OFF
Select TRIGGER MODE		
Set:	AUTO	ON

b. Connect the sine wave output of the appropriate generator through a 50-Ω cable, a 5X attenuator, a 50-Ω terminator (install terminator between the 5X attenuator and the Dual-Input Coupler) and a Dual-Input Coupler to the CH 1 and the EXT TRIG 1 input connectors. Use the Function Generator (item 5) for Test Frequencies below 50 MHz, the Primary Leveled Sine-wave Generator (item 1) for the 50 MHz Test Frequency, and the Secondary Leveled Sine-wave Generator for the 300 MHz Test Frequency (when using the secondary generator, substitute the generator's leveling head for the 50-Ω cable in the test setup).

c. Select TRIGGER SOURCE and push the EXT menu button. Set A EXT SOURCE 1¦2 to 1.

d. Press the A/B TRIG button to select the B Trigger System (the B TRIG SOURCE menu will be displayed). Push the EXT menu button and set B EXT SOURCE 1¦2 to 1. Press the A/B TRIG button to return to the A Trigger System.

e. Adjust the generator's output frequency to the first Test Frequency setting specified in Table 4-4.

f. Set the A SEC/DIV control to the setting used with that Test Frequency.

g. Set the CH 1 VOLTS/DIV control to the setting used with that Test Frequency setting.

h. Select TRIGGER CPLG to display the A COUPLING menu.

Table 4-4

Minimum Signal Level for EXT1 or EXT2 Triggering
(in millivolts)

Trigger System	Test Frequency	VOLTS/DIV Setting	SEC/DIV Setting	TRIGGER COUPLING				
				DC	AC	NOISE REJ	HF REJ	LF REJ
A	60 Hz	5 mV	10 ms	17.5	17.5	[a]	[a]	(17.5)[b]
B	60 Hz	5 mV	10 ms	35.0	35.0	[a]	[a]	(35.0)[b]
A	30 kHz	5 mV	20 μs	17.5	17.5	[a]	25	[a]
B	30 kHz	5 mV	20 μs	35.0	35.0	[a]	50	[a]
A	80 kHz	10 mV	10 μs	17.5	17.5	[a]	[a]	25
B	80 kHz	10 mV	10 μs	35.0	35.0	[a]	[a]	50
A	50 MHz	10 mV	20 ns	17.5	17.5	60	(60)[b]	25
B	50 MHz	10 mV	20 ns	35.0	35.0	120	(120)[b]	50
A	300 MHz	50 mv	2 ns	50.0	50.0	150	(150)[b]	50
B	300 MHz	50 mV	2 ns	100.0	100.0	300	(300)[b]	100

[a]Not necessary to check.
[b]Not triggered at specified amplitude.

NOTE

The Minimum Signal Amplitude Level for Triggering for EXT TRIG÷5 are 5X the levels that are listed in Table 4-4. This procedure obtains the 5X levels by removing a X5 attenuator from the test setup after setting the generator's output level as specified in Table 4-4.

i. Set the output amplitude of the specified Test Frequency to the level given in Table 4-4 for the A Trigger System with DC Trigger Coupling.

NOTE

When checking for triggers in part j, use the TRIGGER LEVEL control to trigger (or to attempt to trigger) on the waveform.

j. CHECK—For a stable, triggered display at the DC trigger coupling setting. Press TRIGGER SLOPE to check for both + and − slopes.

k. Remove the 5X attenuator from the test setup and reconnect the setup as in part b.

l. Set CH 1 VOLTS/DIV for an on-screen display.

m. Select TRIGGER SOURCE and push the EXT menu button. Set A and B EXT GAIN to EXT 1/5 on in the menu displayed.

n. Select TRIGGER CPLG and repeat part j to check A EXT/5 coupling.

o. If trigger sensitivity was near the specified limits for the EXT 1 or EXT/5 sources with the trigger coupling set to DC on, repeat parts i through n for all other coupling settings in that test frequency row, changing the trigger coupling settings and generator amplitude as required.

p. Set the generator's output to the next Test Frequency in Table 4-4.

q. Select TRIGGER SOURCE and push the EXT menu button. Set A and B EXT GAIN back to EXT 1 in the menu displayed. Reinstall the 5X attenuator in the test setup.

r. Repeat parts f through q to check the trigger sensitivity for each test frequency in Table 4-4. Change generators (as specified in part b) as needed to obtain the test frequency required.

s. Move the leg of the Dual-Input-Connector connected to the EXT 1 input to the EXT 2 input.

t. Select TRIGGER SOURCE and push the EXT menu button. Set the A EXT SOURCE 1:2 TO 2. Select TRIGGER COUPLING.

u. Repeat parts e through r to check the EXT 2 trigger source, setting EXT 2/5 and EXT 2 in parts m and q, respectively.

v. Select TRIGGER SOURCE and set VERT on (the VERT source will ensure that the A Acquisition System is stably triggered—required for the following B Trigger checks).

w. Press A/B TRIG to select the B Trigger System and set the HORIZONTAL MODE to B.

x. Repeat parts b to u to check B Trigger System sensitivity. Use generator amplitude levels in the TRIGGER SYSTEM—B rows for checking the B Trigger sensitivity.

NOTE

When checking 50-MHz and 300-MHz Triggers for the B TRIGGER SYSTEM, the REPET mode acquisitions can require a long time to complete. When setting the B SEC/DIV control for those TEST FREQUENCIES, set the HORIZONTAL MODE to A and set the A SEC/DIV control to the SEC/DIV setting specified in the table. This adjustment will set BOTH A and B Acquisition Systems to the specified SEC/DIV setting and reduce the time necessary to complete the B REPT acquisition sequence. Set the HORIZONTAL MODE back to B.

y. Disconnect the test setup.

3. Check A*B Trigger Source.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set:	A SEC/DIV	10μs
Select TRIGGER MODE		
Set:	AUTO	On
Select TRIGGER SOURCE		
Set:	A*B:WORD	A*B

Press A/B TRIG to display the B TRIG SOURCE menu.

Set:	CHAN 1:2	2

b. Ensure that the B Trigger Level Readout is set to 0.0 V. Adjust if necessary using the TRIGGER LEVEL control.

c. Press the A/B TRIG button to select the A Trigger System.

d. Select VERTICAL MODE and set CH2 off.

e. Connect the output of a Leveled Sine-wave Generator through a 50-Ω cable and a Dual-Input Coupler to the CH1 and CH2 input connectors. Do not use a terminator.

f. Set the generator's frequency to 50 kHz and its amplitude for a 4-division display.

g. Use the TRIGGER LEVEL control to adjust the A Trigger Level Readout while performing parts h through n.

h. VERIFY—That for Trigger Level Readout settings of approximately ≤ 0 V the display is stably triggered with the Trigger indicator (a small "T") approximately centered vertically on the waveform.

i. VERIFY—That for Trigger Level settings between approximately 0 V and 200 mV the display is stably triggered and the Trigger Indicator moves along the upper-positive going slope of the waveform.

j. VERIFY—That for settings greater (more positive) than approximately 200 mV the display is not triggered (free-runs). Press A/B TRIG to select the B Trigger System and set SLOPE to – (negative).

k. Press A/B TRIG to select the A Trigger System and set SLOPE to – (negative).

k. VERIFY—That for Trigger Level Readout settings of ≥ approximately 0 V or more the display is stably triggered with the Trigger indicator approximately centered vertically on the waveform.

m. VERIFY—That for Trigger Level settings between approximately 0 mV and −200 mV the display is stably triggered and the Trigger Indicator moves along the lower-negative going slope of the waveform.

n. VERIFY—That for settings which are less (more negative) than approximately 200 mV the display is not triggered (free-runs).

o. Set the A Trigger Level Readout for a reading of 0.0 V and SLOPE to + (positive).

p. Press A/B TRIG to select the B Trigger System and set SLOPE to + (positive).

q. Repeat parts h through o to verify the B Trigger System as a source for the A*B composite trigger. Do NOT change the HORIZONTAL MODE to B. Note that the Trigger Level Readout will indicate B Trigger Level settings for parts h through o and that performance of part j will select the A Trigger System, while part k will select the B Trigger System.

r. Disconnect the test setup.

4. Verify the Normal and Single Sequence Trigger Functions.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select:	VERTICAL MODE	
Set:	CH2	Off
Set:	A SEC/DIV	10μs

b. Connect the Leveled Sine-wave Generator output to CH1 input through a 50-Ω cable.

c. Set the generator's frequency and amplitude for a 50-kHz, 4-division display.

d. Select TRIGGER MODE and set NORMAL on.

e. Using the TRIGGER LEVEL control, VERIFY that the display can be triggered on the positive going slope of the ac waveform for the + (plus) selection of the SLOPE button and on the negative going slope for the − (minus) selection of the SLOPE button.

f. VERIFY—That for TRIGGER LEVEL settings outside the range of the display (approximately ±200 mV), the acquisition stops and the waveform is saved on screen.

g. Trigger the display and set SINGLE SEQUENCE on.

h. VERIFY—That for each press of the STORAGE ACQUIRE button, a waveform is acquired and saved on screen.

i. Disconnect the test setup.

5. Check Trigger Noise Rejection.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select:	VERTICAL MODE	
Set:	CH2	Off
Set:	A SEC/DIV	10μs

b. Connect the sine wave output of the Function Generator through a 50-Ω cable and a 50-Ω terminator to the CH1 input connector.

c. Set the generator's frequency to 50 kHz and its amplitude for a 4-division display.

d. Change the CH1 VOLTS/DIV to 1 V (yields a 0.4-division display).

e. Select TRIGGER COUPLING and set NOISE REJECT on.

f. CHECK—For a non-triggered, free-running display for both the + (positive) and − (negative) settings of the SLOPE button.

g. Set the A COUPLING menu back to DC on.

h. Press the A/B TRIG button to select the B Trigger System (the B COUPLING menu will be displayed) and set the HORIZONTAL MODE to B.

i. Set the B COUPLING menu to NOISE REJECT on.

j. CHECK—That the display cannot be stably triggered with the TRIGGER LEVEL control for either positive or negative setting of the SLOPE button.

k. Set the B COUPLING menu to DC on and disconnect the test setup.

6. Check Slope Selection and Verify Line Trigger.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH2 Off

Select CH1 COUPLING/INVERT
Set: 50Ω ON:OFF OFF

Set: CH1 VOLTS/DIV 5V
A SEC/DIV 5ms

Select: TRIGGER SOURCE
Set: LINE On

CAUTION

DO NOT connect the probe ground lead to the ac (line) power source when performing this step.

b. Connect a 10X probe to the CH1 input connector and connect the probe tip to an ac (line) source.

c. Using the TRIGGER LEVEL control, VERIFY that the display can be triggered on the positive going slope of the ac waveform for the + (plus) selection of the SLOPE button and on the negative going slope for the − (minus) selection of the SLOPE button.

NOTE

The Trigger Point Indicator, a small "T" riding on the displayed waveform, indicates the point on which the instrument is triggered for the displayed waveform.

d. Disconnect the test setup.

7. Verify A and B Trigger Position Function.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH2 Off

Set: CH1 VOLTS/DIV 1V

b. Connect the MARKER output of the Time Mark Generator to the CH1 input through a 50-Ω cable.

c. Set the generator's marker period to 1 ms.

d. Position the start of the display to the extreme left graticule line.

e. Select TRIG POSITION and set 1/8 on.

f. VERIFY—That the Trigger Point Indicator (a "T" symbol on screen) is positioned on a time marker approximately 2.5 divisions to the right of the extreme left graticule line.

g. Set the TRIGGER POSITION menu to 1/4 and verify that the Trigger Point Indicator moves to a time marker that is approximately at center screen.

h. Use the HORIZONTAL POSITION control to position the time marker with superimposed Trigger Point Indicator to the extreme left graticule line.

i. Set the TRIGGER POSITION menu to 1/2 and verify that the Trigger Point Indicator moves to a time marker that is approximately at center screen.

j. Use the HORIZONTAL POSITION control to position the time marker with superimposed Trigger Point Indicator to the extreme left graticule line.

k. Set the TRIGGER POSITION menu to 3/4 and verify that the Trigger Point Indicator moves to a time marker that is approximately at center screen.

l. Set the TRIGGER POSITION menu to 7/8 and verify that the Trigger Point Indicator is positioned on a time marker approximately 2.5 divisions to the right of the center graticule line.

m. Press A/B TRIG to select the B Trigger System and set the HORIZONTAL mode to B. Use the TRIGGER LEVEL control to trigger the display as required.

n. Repeat parts d through k to check the B TRIGGER POSITION function.

o. Disconnect the test setup.

HORIZONTAL SYSTEM

EQUIPMENT REQUIRED (see Table 4-1)

Time-Mark Generator (Item 4)	Termination (Item 12)
Coaxial Cable (Item 10)	10X Probe (Item 16)
Precision Coaxial Cable (Item 11)	1X Probe (Item 17)

1. Check Cursor Readout Accuracies for the A and B Acquisition Systems.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set:	CH1 VOLTS/DIV	1V
	CH2 VOLTS/DIV	2V

Select CURSOR FUNCTION

Set:	TIME	On

b. Use the CURSOR/DELAY control to align the movable cursor (it will have more dots than the alternate cursor) to the third graticule line to the left of center screen.

c. Press CURSOR SELECT to enable the alternate cursor.

d. Use the CURSOR/DELAY control to align cursor to the third graticule line to the right of center screen.

e. CHECK—That the Cursor Time Readout indicates 2.9700 to 3.0300 ms.

f. Set the HORIZONTAL MODE to B.

g. CHECK—That the Cursor Time Readout indicates 2.9700 to 3.0300 ms.

2. Verify the Sample Rate of the A and B Acquisition Systems and Check the Horizontal Display Accuracy.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE

Set:	CH2	Off

Set:	CH1 VOLTS/DIV	500mV
	A SEC/DIV	100ns
	A/B TRIG	B

b. Connect the MARKER OUT signal of a Time Mark Generator to the CH1 input through a 50-Ω cable. Do not use a terminator.

c. Set the generator's marker period to 0.1 μs.

d. Push INIT @ 50% to set the B Trigger level.

e. VERIFY—That one time marker per horizontal division is displayed.

f. CHECK—That the spacing between the time markers nearest the third and ninth vertical graticule lines is 6 divisions, ±0.06 division.

g. Set HORIZONTAL MODE to B and set the B SEC/DIV control to 100 ns.

h. VERIFY—That one marker per horizontal division is displayed.

i. CHECK—That the spacing between the time markers nearest the third and ninth vertical graticule lines is 6 divisions, ±0.06 division.

j. Rotate the A and B SEC/DIV control counterclockwise one position to set both acquisition systems one speed slower.

k. Set the generator's marker period to match the acquisition rate set in the last part.

l. VERIFY—That one marker per horizontal graticule line is displayed.

m. CHECK—That the spacing between the time markers nearest the third and ninth vertical graticule lines is 6 divisions, ±0.06 division.

n. Set HORIZONTAL MODE to A.

o. VERIFY—That one marker per horizontal division is displayed.

p. CHECK—That the spacing between the time markers nearest the third and ninth vertical graticule lines is 6 divisions, ±0.06 division.

q. Set HORIZONTAL MODE to B.

r. Repeat parts j through q to verify all A and B acquisition rate settings down to 500 ms.

s. Disconnect the test setup.

3. Verify the DELAY TIME and Δ DELAY TIME Functions, Check Δ DELAY TIME Resolution, and Check Accuracy of the Time-Base Reference (using the Δ DELAY TIME function).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select:	VERTICAL MODE	
Set:	CH2	Off
Set:	CH1 VOLTS/DIV	500mV
	A SEC/DIV	20μs
	HORIZONTAL MODE	A INTEN
	B SEC/DIV	500ns
	A/B TRIG	B

b. Select TRIGGER MODE and set RUNS AFTER on. Set A/B TRIG to A.

c. Use the HORIZONTAL POSITION control to align the Trigger Point Indicator (a small "T" on the displayed trace) to the vertical graticule line 3 divisions left of center screen.

d. Connect the MARKER OUT signal of a Time Mark Generator to the CH1 input through a 50-Ω cable. Do not use a terminator.

e. Set the generator's marker period to 20 μs. Vertically position the bottom of the CH 1 display to 1 division below center screen.

f. Select DELAY TIME and use the CURSOR/DELAY control to adjust the DELAY TIME Readout for a reading of 120.00 μs.

g. VERIFY—That the intensified zone is on the time marker that is 3 divisions right of center screen.

h. Set the HORIZONTAL MODE to B. VERIFY—the B Trigger Point Indicator is on the rising edge of the displayed time marker.

i. Set the HORIZONTAL MODE to A INTEN and use the HORIZONTAL POSITION control to position the A Trigger Point Indicator to the graticule line 4 divisions left of center screen.

j. Use the CURSOR/DELAY control to adjust the DELAY TIME Readout for a reading of 20.00 μs (the intensified zone will be aligned to the time marker 3 divisions left of center screen).

k. Press the Δ TIME ON/OFF menu button to set Δ TIME ON.

l. Using the CURSOR/DELAY control, adjust the Δ DELAY TIME Readout for a reading of 120.00 μs.

m. VERIFY—That the Δ DELAY intensified zone is on the marker 3 divisions right of center screen.

n. Slightly rotate the CURSOR/DELAY control to increase the Δ DELAY TIME reading the least amount possible.

o. CHECK—That the readout can be advanced in increments at least as small as 0.04 μs.

p. Rotate the CURSOR/DELAY control to set the Δ DELAY TIME readout to 500 μs.

q. Set the HORIZONTAL MODE to B, then set the B SEC/DIV control to 5 ns.

r. Use the HORIZONTAL POSITION control to align the two Trigger Point Indicators to the center vertical graticule line.

s. CHECK—That the two time markers displayed are not horizontally separated by more than 1.5 divisions at the points where their rising edges cross the center horizontal graticule line.

t. Disconnect the test setup.

4. Verify the DELAY EVENTS function.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select CH2 COUPLING/INVERT		
Set:	50Ω ON|OFF	OFF
Set:	CH1 VOLTS/DIV	1V
	CH2 VOLTS/DIV	2V
	A SEC/DIV	5ms
	A/B TRIG	B

b. Select TRIGGER MODE and set RUNS AFTER on. Set A/B TRIG to A.

c. Connect the MARKER OUT signal of a Time Mark Generator to the CH1 input through a 50-Ω cable. Do not use a terminator.

d. Set the generator's marker period to 5 ms.

e. Connect the A TRIG (TTL) output at the scope's rear panel to the CH2 input connector with a 50-Ω BNC cable. Do not use a terminator.

f. Use the VERTICAL POSITION controls to position the CH1 and CH2 displays for easy viewing.

g. Select TRIGGER SOURCE and push the EXT menu button. Set A AND B EXT to EXT1/5.

h. Press the A/B TRIG button to select the B Trigger System.

i. Select TRIGGER SOURCE and push the EXT menu button. Set B EXT SOURCE 1\|2 to 1. Press the A/B TRIG button to return to the A Trigger System.

j. Connect the output of a Leveled Sine-wave Generator to the EXT TRIG 1 input via a 50-Ω BNC cable and a 50-Ω terminator.

k. Set the Leveled Sine-wave Generator's amplitude to 3 volts and its frequency to 2 MHz.

l. Set the HORIZONTAL MODE to B and set the B SEC/DIV control to 50 μs.

m. Use the HORIZONTAL POSITION control to align the Trigger Point Indicators to the graticule line 3 divisions right of center screen.

n. Set the HORIZONTAL MODE to A.

o. Select DELAY EVENTS and set EVENTS ON\|OFF to ON. Use the CURSOR/DELAY control to set the EVENTS COUNT to 60001 B TRIGS.

p. VERIFY—That the falling edge of the A Trigger signal displayed in CH2 is 3 divisions left of center screen.

q. Set the HORIZONTAL MODE to B.

r. VERIFY—That the rising edge of the displayed time marker can be aligned to the Trigger Point Indicator approximately 3 divisions right of center screen using the CURSOR/DELAY control.

s. Disconnect test setup.

ADDITIONAL VERIFICATIONS AND CHECKS

NOTE

Items 20 and 22 through 24 are only needed to check instruments equipped with the Video Option (Option 05). Item 21 is needed to check both the standard instrument and the option 5 instrument.

EQUIPMENT REQUIRED (see Table 4-1)

Calibration Generator (Item 3)
Digital Voltmeter (DMM) (Item 7)
GPIB Controller (Item 8)
GPIB Interface Cable (Item 9)
Coaxial Cable (Qty 2) (Item 10)
Termination (Item 12)
10X Attenuator (Qty 2) (Item 13)
1X Probe (Item 17)
BNC Female-to-Dual Adapter (Item 19)
Sine-Wave Oscillator (Item 20)
Pulse Generator (Item 21)
Sync and Linearity Test Generator (Item 22)
Coaxial Cable (Qty 2) (Item 23)
Termination (Qty 2) (Item 24)

1. Check Gain Match Between NORMAL and Save Acquisition Modes.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select CH1 COUPLING/INVERT		
Set:	50Ω ON:OFF	OFF
Select STORAGE ACQUIRE		
Set:	AVG	On
Select VERTICAL MODE		
Set:	CH 2	Off

b. Connect the Calibration Generator's STD AMPLITUDE output to the CH1 input connector. Set the generator's output level to .5 V and center the displayed square wave on screen.

c. Select CURSOR FUNCTION and set VOLTS on.

d. Using the CURSOR/DELAY control, align the enabled cursor (segmented) to the top of the displayed square wave.

e. Press CURSOR SELECT to enable the alternate cursor (it will change from solid to segmented). Align the cursor to the bottom of the square wave.

f. Note the CURSOR VOLTS readout value.

g. Select STORAGE SAVE to save the display. Realign the cursors to the saved square wave if required.

h. CHECK—That the CURSOR VOLTS readout value is within 12 mV of the value noted in part f.

i. Disconnect the test setup.

2. Verify the Cursor Units and Functions.

NOTE

This check VERIFIES the functionality of the cursors. The accuracy of the cursor readout is checked in the Vertical and Horizontal Systems subsections of this procedure.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE		
Set:	CH2	Off
Select CH1 COUPLING/INVERT		
Set:	50Ω ON¦OFF	OFF
Select TRIGGER MODE		
Set:	AUTO	On
Select CURSOR FUNCTION		
Set:	TIME	On

b. Use the CURSOR DELAY control to align the enabled time cursor to the vertical graticule line 2 divisions left of center screen.

c. Press the CURSOR SELECT button to enable the alternate cursor (realign the Trigger Point Indicator (small "T") to center screen (if necessary) and align it to the graticule line 2 divisions right of center screen.

d. VERIFY—That the cursor readout indicates approximately 2.00 ms.

e. Select CURSOR UNITS and set Δ¦ABS to ABS. VERIFY—That the cursor readout indicates approximately 1.00 ms.

f. Return Δ¦ABS to Δ and set DEGREES on. Press the NEW REF menu button.

g. VERIFY—That the cursor readout indicates approximately 360.00° and that TIME CURSOR REF = indicates approximately 2.00 ms.

h. Set Δ¦ABS to ABS. VERIFY—That the cursor readout indicates approximately 180.00°.

i. Set % on. VERIFY—That the cursor readout indicates approximately 50.00%.

j. Set SEC on and Δ¦ABS to Δ.

k. Select CURSOR FUNCTION and set 1/TIME on. VERIFY—That the cursor readout indicates approximately 500.00 Hz.

l. Set VOLTS on. Select CURSOR UNITS and set dB on.

m. Use the CURSOR DELAY control to align one volt cursor to the graticule line 2 divisions above center screen and the other volt cursor to the line 2 divisions below center screen. Use the CURSOR SELECT button to toggle between cursors.

n. Press the NEW REF menu button. VERIFY—That the cursor readout indicates 0.0 dB.

o. Align the enabled cursor to the center horizontal graticule line. VERIFY—That the cursor readout indicates approximately −6.00 dB.

p. Connect the CALIBRATOR signal to the CH1 input connector through a X1 probe.

q. Vertically center the display (do not position horizontally). Use the TRIGGER LEVEL control to trigger the display.

r. Set the CURSOR UNITS menu to VOLTS and select the CURSOR FUNCTION menu. Set V@T on.

s. Position one time cursor to 1 division left of center screen; position the other time cursor to 1 division right of center screen. VERIFY—That the cursor readout indicates approximately 400.00 mV.

t. Set the CURSOR FUNCTION menu to SLOPE. VERIFY—That the cursor readout indicates approximately 400.00 V/s.

u. Disconnect test setup.

3. Verify STORAGE SAVE Functions.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select TRIGGER MODE
Set: AUTO On

b. Use the VERTICAL POSITION controls to position the CH 1 trace 2 divisions above graticule center and the CH 2 trace 2 divisions below graticule center.

c. Select VERTICAL MODE and set ADD on (ADD trace will be at graticule center).

d. Select STORAGE SAVE and press the menu button labeled CH1 (the menu will change from SAVEREF SOURCE to SAVEREF DESTINATION).

e. Press the menu button labeled REF1 (the menu will change back to SAVEREF SOURCE). Press CH2, REF2, ADD, REF3, REF, REF1, and REF4 in that order (menu will change for each button push) to store CH2 in REF2, ADD in REF3, and REF1 in REF4.

f. Select VERTICAL MODE and set CH1, CH2, and ADD off.

g. Select STORAGE DISPLAY REF and press the REF1, REF2, and REF3 buttons. VERIFY—That the REF1 trace is displayed 2 divisions above, the REF2 trace 2 divisions below, and the REF3 trace at center screen.

h. Press the HORIZ POS REF menu button (menu will change) and set REF1 on for the displayed menu. VERIFY—That the HORIZONTAL POSITION control can position the REF1 trace horizontally. Repeat verification for REF2 and REF3.

i. Set REF HPOS REF!LOCK to LOCK. VERIFY—That the HORIZONTAL POSITION control now positions all displayed REF traces simultaneously.

j. Press the DISPLAY REF menu button to return to that menu. Set REF1 off and REF4 on. VERIFY—That the REF4 trace replaces the REF1 trace.

4. Verify Auto Setup.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH2 Off

Select: CH 1 COUPLING/INVERT
Set: 50Ω ON!OFF Off

Select: CH 2 COUPLING/INVERT
Set: 50Ω ON!OFF Off

b. Connect the output of a pulse generator to the CH 1 and CH 2 inputs through a 50-Ω cable, a 10X attenuator, and a dual-input coupler.

c. Set the CH 1 VOLTS/DIV to 100 mV and the A SEC/DIV to 20 μs.

d. Set the generator's output for a 500 mV pk-pk amplitude with the peak levels ±250 mV around the ground indicator ("+", at the left side of the screen).

e. Set the generator period for 100 μs (5 divisions) and the pulse duration (positive duration) for approximately 25 μs (1.25 divisions).

f. Push the front-panel button labeled AUTO to do an Auto Setup on the input waveform for CH 1.

g. VERIFY—That the scope displays the Auto Setup menu and the message "AUTOSETUP WORKING: PLEASE WAIT" as it acquires information about the CH 1 waveform.

h. VERIFY—That the Auto Setup mode is VIEW (from the recalled front-panel setup).

i. VERIFY (after the message is removed)—That several cycles of the Channel One cycle are displayed centered vertically on screen. The display amplitude should be approximately 5 divisions, and the Trigger Point Indicator (a small "T", riding on the waveform) should be at center screen.

j. Set the input coupling to AC in the CH 1 COUPLING/INVERT menu to remove the average dc component from the waveform and create waveform with DC offset from ground (that is, one not centered vertically around ground).

k. Push AUTO. VERIFY—That the scope sizes the waveform to handle the offset by increasing the VOLT/DIV setting. The display amplitude should be about 2.5 divisions on screen.

l. Return the CH 1 coupling to DC.

m. Select VERTICAL MODE and set CH 2 on.

n. Push AUTO. VERIFY—That the scope scales both the CH 1 and CH 2 waveforms and positions the CH 1 waveform to the top half of the screen and the CH 2 waveform to the bottom half. The amplitude of each display should be about 2.5 divisions.

o. Set the Auto Setup MODE to PERIOD. VERIFY—that the menu entry RES HI:LO appears with the setting LO.

p. Select VERTICAL MODE and set CH 2 back off.

q. Push the AUTO button. VERIFY—That between 1 and 2 cycles of the waveform are displayed on screen. The amplitude should be about 2.5 divisions and the Trigger Point Indicator should be near the beginning of the 20-division waveform record. The trigger slope should be positive.

r. Set the input coupling to AC in the CH 1 COUPLING/INVERT menu to remove the average dc component from the waveform and create waveform with DC offset from ground.

s. Push AUTO. VERIFY—That the scope handles DC offset by positioning the ground indicator ("+") down about ½ division below center screen.

t. Set RES HI:LO to HI in the Auto Setup menu.

u. Return the CH 1 coupling to DC.

v. Push AUTO. VERIFY—That the waveform is displayed with about a 5-division amplitude, with about 1-2 cycles included in the ENTIRE 20-division waveform record. Use the HORIZONTAL POSITION control to view the entire waveform. The waveform should be triggered on the positive slope with the Trigger Point Indicator near the beginning of the record.

w. Set the RES (Resolution) back to LO and the Auto Setup mode to PULSE.

x. Push AUTO. VERIFY—That the positive ¼-cycle of the waveform is displayed on screen. The amplitude is about 2.5 divisions, and the trigger point is near the beginning of the record, triggered on the positive slope.

y. Set the generator to produce a COMPLEMENT pulse; that is, one with a negative ¼-cycle pulse duration.

z. Push AUTO. VERIFY—That the negative ¼-cycle of the waveform is displayed on screen. The amplitude is about 2.5 divisions, and the trigger point is near the beginning of the record, triggered on the negative slope.

aa. Set the RES to HI.

bb. Push AUTO. VERIFY—That the negative ¼-cycle of the waveform is displayed over about 10 of the 20 divisions in the waveform record. The amplitude is about 5 divisions, and the trigger point is near the beginning of the record, triggered on the negative slope.

cc. Set the RES to LO and the mode to _/‾.

dd. Push AUTO. VERIFY—That the positive-going (rising) edge of the waveform is displayed on screen with the Trigger Indicator at center screen. Waveform amplitude is about 2.5 divisions.

ee. Set the MODE to ‾_.

ff. Push AUTO. VERIFY—That the falling (negative-going) edge of the waveform is displayed on screen with the Trigger Indicator at center screen. Waveform amplitude is about 2.5 divisions.

gg. Set the RES to HI.

hh. Push AUTO. VERIFY—That the falling (negative-going) edge of the waveform is displayed over about 10 of the 20 divisions in the waveform record with the same triggering as for RES LO setting. Waveform amplitude is about 5 divisions.

ii. Disconnect the test setup.

5. Verify MEASURE for SNAPSHOT and Continuous-Update Modes.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE		
Set:	CH2	Off
Select: CH 1 COUPLING INVERT		
Set:	50Ω ON¦OFF	Off
Select: CH 1 COUPLING INVERT		
Set:	50Ω ON¦OFF	Off

b. Connect the STD OUTPUT of the Calibration Generator to the CH 1 and CH 2 waveforms via a 50-Ω cable and a dual-input coupler.

c. Set the output of the generator to .5 volts.

d. Push AUTO to do an Auto Setup on the CH 1 waveform. Since AUTOsetup executed in VIEW mode, there should be several cycles of the square wave displayed on screen.

e. Set the AUTOsetup mode to PERIOD and push AUTO.

f. Push MEASURE (next to PRGM, which is right of AUTO) to display that menu.

g. Push SETUP in the menu and set METHOD to HIST and MARK to ON.

h. Press MEASURE again and then SNAPSHOT. VERIFY—That the SNAPSHOT menu is displaying values for 20 parameters approximately agreeing with the expected values. For instance, P-P (peak-to-peak) and TOP should be about 500 mV, and DUTY (duty cycle) should be about 50%.

i. Set the generator to .2 V.

j. Press the INIT@50% front-panel button (located in the TRIGGER section of the controls) to trigger the display.

k. Push AGAIN. VERIFY—That SNAPSHOT readou updates the parameters (P-P and TOP are now abou 200 mV).

l. Set CH 2 on in the VERTICAL MODE menu (leave CH 1 on). Set the CH 2 VOLT/DIV to the same setting as CH 1.

m. Select MEASURE and push SNAPSHOT. Push CH 2 in the TARGET menu displayed.

n. VERIFY—That the parameter values are now displayed for CH 2 (screens read "SNAPSHOT OF CH2").

o. Push the upward-arrow menu button to return to the main MEASURE menu.

p. Set CH 2 off in the VERTICAL MODE menu.

q. Push MEASURE and set WINDOW ON.

r. Push MEAS TYPE and use the direction arrows in the displayed menu to move the underline to PK-PK and press the on button to display the parameter. Repeat for BASE, FREQ, and PERIOD. VERIFY—That as each is turned on the value displayed approximately agrees with the expected values (200 mV, 0 V, 1 kHz, and 1 ms, respectively).

s. VERIFY—That two X's (MARKs) bracket one cycle of the squarewave to indicate where FREQ and PERIOD are being measured (MARKs are displayed for time measurements only).

t. Push CURSOR FUNCTION and set TIME on in the menu displayed.

u. Use the CURSOR/DELAY knob to adjust the active cursor to the center of one positive ½-cycle of the waveform.

v. Push CURSOR SELECT to select the alternate cursor. Adjust it to the center of the following negative ½-cycle of the waveform.

w. VERIFY—That the BASE and PK-PK values displayed are still approximately correct, but the values for FREQ and PERIOD are replaced with the message "NEED 3 EDGES".

x. Adjust the active cursor to the same ½-cycle as the other cursor. VERIFY—That the PK-PK value drops to approximately 0 volts.

y. Use the CURSOR/DELAY and SELECT controls to bracket slightly more than one cycle (3 EDGES) of the waveform. All 4 parameters should be as verified in part r.

z. Disconnect the test setup.

6. Verify Operation of the AutoStep Sequencer.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select:	VERTICAL MODE	
Set:	CH2	Off
Set:	A SEC/DIV	50 ms

b. Press the PRGM front-panel button. VERIFY—The AUTOSTEP SEQUENCER menu is displayed.

c. Press the SAVE menu button. This calls up a submenu for labeling the front-panel setup with a 1-6 character name so it can be recalled later.

d. VERIFY—That a sequence can be labeled and that label saved by doing the following:

Use the arrows under ROLL-CHARS to create a label (use TEST1) for the front-panel setup as outlined here in steps a-d:

1. Select the first character for the label. Use the arrow-labeled buttons to select the first letter for the sequence label. Press the ↓ button to step forward in the alphabet and digit (0-9) and the ↑ button to step backwards. Holding down the buttons moves through the character continuously; a single press moves forward or backward one character. (There is a "blank space" character between the digit 9 and letter A.)
2. When you have displayed the letter for the first character of the label, push CURSOR <> to move to the next character. Repeat part 1 to select the letter for the next character of your label.
3. Repeat the last step until "TEST1" is spelled out. (You can return to any character by continually pushing CURSOR <>, since it reverses the selection order after the first and sixth character is selected.)

e. Push menu button labeled SAVE when the label is complete.

f. VERIFY—That, when SAVE is pushed, the scope displays a message indicating "SEQUENCE TEST1 STEP 1" and the remaining memory in percent.

g. Position the CH 1 trace to the graticule line 3 divisions above graticule center. Push PRGM to advance to sequencer step 1 actions.

h. VERIFY—That the SET STEP ACTIONS for Step 1 is displayed.

i. Use the arrow buttons to move the underline to the "<N>" following the ACTION called REPEAT. Push Y\N to toggle the action to Y ("Y" stands for Yes or On).

j. Now move the underline to the ACTION called BELL, and turn BELL on (set to Y). Using the same procedure, turn PAUSE on also.

k. Push NEXT STEP. VERIFY—That the on-screen message indicates STEP 2.

l. Position the CH 1 trace to the graticule line 1 division above graticule center. Push PRGM to advance to sequencer step 2 actions.

m. VERIFY—That REPEAT, PAUSE, and BELL are the only actions on.

n. Push Y\N to turn REPEAT off. Push NEXT STEP.

o. The message should now say STEP 3. Position the CH 1 trace to the graticule line 1 division below graticule center. Push PRGM to advance to sequencer step 3 actions.

p. PAUSE and BELL are the only actions on. Push NEXT STEP to advance to sequencer step 4.

q. Position the CH 1 trace to the graticule line 3 divisions below graticule center. Push PRGM to advance to sequencer step 4 actions. PAUSE and BELL should be the only action on.

r. Push SAVE SEQ to save the sequence. VERIFY—That the main AUTOSTEP SEQUENCER menu is returned and the message "SEQUENCE SAVED" is displayed.

s. Push RECALL to display the menu for recalling sequences. VERIFY—That TEST1 appears in the list of CURRENT SEQUENCES.

t. Use the arrow buttons to move the underline (select) TEST1.

u. Push RECALL. VERIFY—That the BELL rings and the setup stored as step 1 is displayed. The CH 1 trace should be located 3 divisions above graticule center.

v. Push PRGM (front-panel button). VERIFY—That the BELL rings and the setup stored as step 2 is displayed. The CH 1 trace should be located 1 division above graticule center.

w. Push PRGM. VERIFY—That the BELL rings and the setup stored as step 3 is displayed. The CH 1 trace should be located 1 division below graticule center.

x. Push PRGM. VERIFY—That the BELL rings and the setup stored as step 4 is displayed. The CH 1 trace should be located 3 divisions below graticule center.

y. Push PRGM. VERIFY—That the BELL rings and the sequence loops back to display step 1 of the sequence.

z. Connect the STEP COMPLETE output BNC (rear panel) to the banana plug inputs of a DMM via a 50-Ω cable and a BNC female-to-banana adapter. When connecting the adapter to the DMM, put the side with the bump marked "GRD" to the LOW or (—) input jack.

aa. Set the DMM to the 20 DC VOLT range. CHECK—That the DMM reading is ≤ 0.5 V.

bb. Push PRGM to advance to sequence step 2. CHECK—That the DMM reading momentarily jumps to a level ≥ 2.5 V and ≤ 3.5 V before returning to the level measured in subpart aa.

cc. Move the 50-Ω cable from the STEP COMPLETE output to the SEQ OUT output BNC. CHECK—That the DMM reading is ≥ 2.5 V and ≤ 3.5 V.

dd. Push PRGM once to advance to sequence step 3. Wait until step 3 is loaded and then push PRGM again to advance to step 4.

ee. CHECK—That the DMM reading is ≤ 0.5 volts.

ff. Connect the square wave output of a generator (such as Item 19) capable of outputting nominal TTL levels to the SEQ IN input via a 50-Ω cable. Set the output frequency of the generator to 10 Hz.

gg. VERIFY—That the scope continuously loops through sequencer steps 1 to 4 in response to the generator input.

hh. Push EXIT. VERIFY—That the RECALL menu is returned.

ii. Push EXIT. VERIFY—That the main AUTOSTEP SEQUENCER menu is returned.

7. GPIB Functionality Verification.

NOTE

Verification Step 7 assumes a TEKTRONIX 4041 Controller will be used for verifying GPIB Functionality. Examples of Talk-Listen Programs for some other controllers can be found in the Programmers Reference Guide included with this instrument. Users will have to adapt this verification step for use with controllers other than the TEKTRONIX 4041.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure).

b. Select OUTPUT (the button to the lower right of SEC/DIV control) and press the menu button labeled SETUP (menu will change).

c. Press the menu button labeled MODE to display that menu.

d. Set T/L on. VERIFY—That the ADDR light is off.

e. Set L/ONLY on. VERIFY—That the ADDR light is on.

f. Set T/ONLY on. VERIFY—That the ADDR remains on. Set the mode back to T/L.

g. Select OUTPUT and press the menu button labeled SETUP.

h. Press the menu button labeled ADDR to select that menu.

i. Press the menu button labeled ↑ or ↓ to set the GPIB ADDRESS to 1. The ↑ increments the address and the ↓ decrements it.

j. Select OUTPUT and press the menu button labeled SETUP. Press the menu button labeled TERM (menu will change).

k. Set either EOI or LF/EOI on according to the specification of the controller.

l. Turn on the controller and enter a program that can deliver commands and queries to, as well as receive response from the scope.

m. Connect the GPIB controller to the oscilloscope's rear-panel GPIB CONNECTOR using the GPIB cable.

n. Run the program entered for subpart l.

o. Enter 1 in response to the controller's prompt for the oscilloscope's address (the controller may or may not issue an error code and event number in response).

p. Enter the command RQS ON.

q. Press the instrument's POWER button twice to power the instrument OFF and then ON.

r. VERIFY—That all three GPIB STATUS lights illuminate during the instrument's power-up sequence.

s. VERIFY—The GPIB STATUS SRQ light is still illuminated when the power-up sequence is finished.

t. Enter a carriage return at the controller.

u. VERIFY—That the GPIB STATUS SRQ light is no longer illuminated.

v. Enter the command LOCK ON on the controller. VERIFY—That the LOCK light is illuminated.

w. Enter the following commands on the controller:

1. ↓ VMOde ADD!ON
2. CH1 VOLts!1E-1, VARiable—50, POSition:2, COUpling:GND, FIFty:OFF, INVert:ON
3. CH2 VOLts:1E-1, VARiable:50, POSit-2, COUpling:GND, FIFty:OFF, INVert:ON
4. BWLimit TWEnty
5. HORizontal ASEC:1E-3,BSEC:1E-4
6. DLTime DELta:ON,DLY1:1E-3,DLY2:1E-3

x. Enter the command RTL to the controller. VERIFY—That the LOCK light is extinguished.

y. Select BEAMFIND. VERIFY—That front panel STATUS readout indicates the control setting changes sent over the controller in part I have been performed.

z. Press the MENU OFF/EXTENDED FUNCTIONS button.

aa. VERIFY—That the CH1 trace is displayed 2 divisions above the center graticule line with an intensified zone 1 division right of center screen.

bb. VERIFY—That the CH2 trace is displayed 2 divisions below the center graticule line with an intensified zone 2 divisions right of center screen.

cc. Enter the command VMOde? to the controller.

dd. VERIFY—That the controller's display indicates that the oscilloscope's VERTICAL MODE setting is CH1 on, CH2 on, and ADD On.

ee. Disconnect the test setup.

8. Check A TRIGGER and RECORD TRIGGER Outputs for Logic Polarity and Minimum HI/LO (50-Ω loads).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select CH1 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Select CH2 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Set:	CH 1 VOLTS/DIV	200mV
	CH 2 VOLTS/DIV	200mV
Select TRIGGER SOURCE		
Set:	LINE	On

b. Connect the RECORD TRIGGER OUTPUT (rear panel) to the CH 1 input connector via a 50-Ω cable and a 50-Ω terminator.

c. Connect the TRIGGER OUTPUT (rear panel) to the CH 2 input connector via a 50-Ω cable and a 50-Ω terminator.

d. Using the CH 1 and CH 2 VERTICAL POSITION controls, position the CH 1 waveform to the top-half of the screen and the CH 2 to the bottom-half for easy viewing.

e. CHECK—That both of the waveforms are displayed with their falling edges aligned to the Trigger Point Indicator (a small "T" riding on each waveform).

f. Select CURSORS FUNCTION and set VOLTS ON.

g. Select CURSOR UNITS and set Δ!ABS to ABS.

h. Use the CURSOR/DELAY control to align the Voltage cursor to the top flat portion of the CH 1 waveform.

i. CHECK—That the Cursor Readout indicates a voltage ≥ 450 mV.

j. Align the Voltage cursor to the bottom flat portion of the CH 1 waveform.

k. CHECK—That the Cursor Readout indicates a voltage <= 150 mV.

l. Press the CURSOR FUNCTION button twice to display the Attach Cursors menu and set CH 2 on for the displayed menu.

m. Repeat parts h through k, aligning the cursor to the CH 2 waveform instead of the CH 1.

n. Disconnect the test setups.

9. Check Square-Wave Flatness (Video Option 05 only).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select CH1 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Select CH2 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Set:	CH1 VOLTS/DIV	200 mV
	CH2 VOLTS/DIV	50 mV
	A SEC/DIV	2 ms
Select: VERTICAL MODE		
Set:	CH2	Off

b. Connect the fast-rise, positive going square-wave output to the CH1 input connector via a 50-Ω cable and a 50-Ω terminator. The square wave should step from −1 V to 0 V.

c. Set the generator to produce a 60-Hz, five-division display and use the CH1 POSITION control to center the display as required.

d. Set the CH1 VOLTS/DIV control to 50 mV.

e. CHECK—Display front-corner aberrations are within 1% (0.2 division or less). Exclude the first 20 ns immediately following the positive going transition from the measurement.

f. Set CH2 on and CH1 off.

g. Move the cable from the CH1 input connector to the CH2 input connector.

h. CHECK—Display front-corner aberrations are within 1% (0.2 division or less). Exclude the first 20 ns immediately following the positive going transition from the measurement.

i. Set the CH2 VOLTS/DIV control to 5 mV.

j. Install a 10X attenuator between the 50-Ω cable and the terminator and reconnect the setup.

k. CHECK—Display front-corner aberrations are within 1% (0.2 division or less). Exclude the first 20 ns immediately following the positive going transition from the measurement.

l. First set the CH 2 VOLTS/DIV control to 50 mV, then set CH1 on and CH2 off.

m. Move the cable from the CH2 input connector to the CH1 input connector. Set the CH1 VOLTS/DIV control to 5 mV.

n. CHECK—Display front-corner aberrations are within 1% (0.2 division or less). Exclude the first 20 ns immediately following the positive going transition from the measurement.

o. Set the CH1 VOLTS/DIV control to 200 mV and set the A SEC/DIV control to 10 μs.

p. Remove the 10X attenuator and reconnect the test setup.

q. Set the generator to produce a 15-kHz, 5-division display.

r. Repeat parts d through n to check square-wave flatness at 15 kHz.

s. Disconnect test setup.

10. Check Frequency Response Flatness (FULL and 20 MHz BANDWIDTH Modes) (Video Option 05 only).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select CH1 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Select CH2 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Set:	CH1 VOLTS/DIV	10 mV
	CH2 VOLTS/DIV	10 mV
	A SEC/DIV	20 μs
Select: VERTICAL MODE		
Set:	CH2	Off
Select: BANDWIDTH		
Set:	20 MHz	On

b. Connect the output of a Leveled Sine-Wave Generator to the CH1 input connector via a 50-Ω cable, two 10X attenuators, and a 50-Ω terminator.

c. Set the generator to produce a 50-kHz, five-division display.

d. Increase the generator output frequency to 5 MHz and set the A SEC/DIV control to 200 ns.

e. CHECK—Display amplitude is between 4.80 and 5.05 divisions.

f. Set the BANDWIDTH LIMIT menu to FULL. Set the A SEC/DIV control back to 20 μs.

g. Repeat parts c and d.

h. CHECK—Display amplitude is between 4.95 and 5.05 divisions.

i. Increase the generator frequency to 10 MHz and set the A SEC/DIV control to 50 ns.

j. CHECK—Display amplitude is between 4.90 and 5.05 divisions.

k. Increase the generator frequency to 30 MHz and set the A SEC/DIV control to 20 ns.

l. CHECK—Display amplitude is between 4.85 and 5.10 divisions.

m. Set the CH1 VOLTS/DIV control to 50 mV and the A SEC/DIV to 20 μs. Set 20 MHz on for the displayed BANDWIDTH menu.

n. Remove one of the 10X attenuators from the test setup.

o. Repeat parts c through l.

p. Set the CH1 VOLTS/DIV control to 200 mV and the A SEC/DIV control to 20 μs. Set 20 MHz on for the displayed BANDWIDTH menu.

q. Remove the last 10X attenuator from the test setup.

r. Repeat parts c through l.

s. Move the cable from the CH1 input connector to the CH2 input connector. Insert the two 10X attenuators back into the test setup.

t. Select VERTICAL MODE and set CH2 on and CH1 off. Return the A SEC/DIV control to 20 μs.

u. Select BANDWIDTH and set 20 MHz on.

v. Repeat parts c through r using the CH2 VOLTS/DIV control.

w. Disconnect the test setup.

11. Check Video Back-Porch Clamp (CH2 only) (Video Option 05 only).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select CH1 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Select CH2 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Set:	CH1 VOLTS/DIV	500 mV
	CH2 VOLTS/DIV	50 mV
	A SEC/DIV	5 ms
Select TRIGGER SOURCE		
Set:	LINE	On
Select: BANDWIDTH		
Set:	20 MHz	On

b. Connect the output of a Sine-Wave RC Oscillator to the CH2 input connector via a 75-Ω cable.

c. Connect the composite sync output of a Video Sync Generator to the CH1 input connector via a 75-Ω cable and a 75-Ω termination. Select VERTICAL MODE and set CH1 off.

d. Set the oscillator to produce a 60-Hz, six-division display. Slightly adjust the output frequency of the oscillator to stabilize the 60-Hz display.

e. Set the A SEC/DIV control to 100 μs. Select TRIGGER SOURCE and set CH1 on.

f. Select SET VIDEO and set CLAMP ON/OFF to ON and TV LINE on.

g. CHECK—The amplitude of the sine wave is 1 division or less.

NOTE

An easy method of checking the expanded 60-Hz sine wave's amplitude is to observe the vertical "jitter" of the top of the Trigger Point Indicator (a small "T" riding on the sine wave). The top of the "T" should not jitter more than 1 division.

h. Set the CH2 VOLTS/DIV control to 100 mV and the A SEC/DIV control back to 5 ms.

i. Set CLAMP off for the displayed menu. Select TRIGGER SOURCE and set LINE on.

j. Repeat parts d through g.

k. Set the CH2 VOLTS/DIV control to 200 mV and the A SEC/DIV control back to 5 ms.

l. Set CLAMP off for the displayed menu. Select TRIGGER SOURCE and set LINE on.

m. Repeat parts d through g.

n. Disconnect the test setup.

12. Check Back-Porch Clamp Reference (CH2 only) (Video Option 05 only).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select VERTICAL MODE		
Set:	CH1	Off
Set:	CH2 VOLTS/DIV	50 mV
	A SEC/DIV	1 μs
Select: BANDWIDTH		
Set:	20 MHz	On
Select CH2 COUPLING/INVERT		
Set:	50Ω ON/OFF	OFF

b. Connect a 100% modulated, composite video signal to the CH2 input connector via a 75-Ω cable and a 75-Ω termination. Do NOT adjust the CH2 POSITION control.

c. Select SET VIDEO and set CLAMP on.

d. CHECK—That the back-porch level is within 1 division of the center graticule line.

e. Disconnect the test setup.

13. Check Sync Separation (±SLOPE) (Video Option 05 only).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select VERTICAL MODE		
Set:	CH2	Off
Set:	CH1 VOLTS/DIV	50 mV
	A SEC/DIV	2 μs
	TRIGGER SLOPE	– (Minus)
Select: BANDWIDTH		
Set:	20 MHz	On
Select CH1 COUPLING/INVERT		
Set:	50Ω ON/OFF	OFF

b. Connect the square-wave output of a Pulse Generator to the CH1 input connector via a 50-Ω cable and a 50-Ω termination.

c. Set the amplitude for a 3-division pulse, stepping negative from ground.

d. Use the HORIZONTAL POSITION control to position the Trigger Point Indicator (small "T" riding on the waveform) to the vertical graticule line 4 divisions left of graticule center.

e. Adjust the generator's PERIOD control for a 7.5-division (approximately 15 μs) period for the displayed square wave.

f. Adjust the generator's PULSE DURATION control until the negative going portion of the square wave is approximately 1 horizontal division in duration.

g. Switch the A SEC/DIV control to 500 ns.

h. Select CURSOR FUNCTION and set TIME on.

i. Use the CURSOR/DELAY control to align the left-most cursor to the falling edge of the negative going pulse (aligned to the graticule line in part d).

j. Press CURSOR SELECT to select the right-most cursor and adjust it for a readout of 2.000 μs.

k. Adjust the generator's PULSE DURATION until the negative-going portion of the square wave is aligned to the two cursors (i.e., is equal to 2.000 μs).

l. Select TRIGGER CPLG and set VIDEO on.

m. Select SET VIDEO and set TV LINE on.

n. Return the A SEC/DIV control to 2 μs. Press CURSOR SELECT and use the CURSOR/DELAY control to realign the left-most cursor to the falling edge of the pulse.

o. Press CURSOR SELECT and use the CURSOR/DELAY control to adjust the right-most cursor for a readout value of 13.000 μs.

p. Set the CH1 VOLTS/DIV control to 200 mV.

q. Adjust the generator to reduce the PERIOD of the waveform. Reduce the period until the display is stably triggered, but any further decrease in period causes an unstable display.

r. CHECK—That the negative-going edge of the second negative pulse is located between the two cursors.

s. Adjust the generator to return the waveform PERIOD to 7.5 divisions.

t. Select CH1 COUPLING/INVERT and set INVERT ON!OFF to ON. Switch TRIGGER SLOPE to + (plus).

u. Adjust the generator to reduce the PERIOD of the waveform. Reduce the period until the display is stably triggered, but any further decrease in period causes an unstable display.

v. CHECK—That the positive-going edge of the second negative pulse is located between the two cursors.

w. Disconnect the test setup.

14. Check VIDEO Trigger Modes.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select VERTICAL MODE		
Set:	CH2	Off
Set:	CH1 VOLTS/DIV	200 mV
	A SEC/DIV	100 μs
	TRIGGER SLOPE	— (Minus)
Select: BANDWIDTH		
Set:	20 MHz	On
Select CH1 COUPLING/INVERT		
Set:	50Ω ON!OFF	OFF
Select TRIGGER CPLG		
Set:	VIDEO	On
Select SET VIDEO		
Set:	FIELD 1	On

b. Push the front-panel button labeled "MENU OFF/EXTENDED FUNCTIONS" twice to display the Extended Functions menu. Push VIDEO OPT in the menu. Set M!NON/M to M and CNT BOTH!F1 to F1.

c. Connect the composite sync output of a Sync Generator to the CH1 input connector via a 75-Ω cable and a 75-Ω termination.

NOTE

For NTSC composite sync input signals, the first field will have 263 lines, while the second field will have 262. The scope will display the line number in the extreme upper-right corner of the screen and the TVF (TV Field) number immediately to the right of the line number.

d. Adjust the TRIGGER LEVEL control for a line number reading of 1 and a field number reading of TVF1.

e. CHECK—That for the readout Trigger Point Indicator (a small "T" riding on the displayed waveform) indicates the scope is triggered on the first line of field 1.

f. Rotate the TRIGGER LEVEL control slightly counterclockwise while performing the CHECK during the following part.

g. CHECK—That the readout indicates the highest line number of the previous field for the multi-field input signal. For example, using an NTSC signal, the readout should indicate "TVF2 262".

h. CHECK—That the readout Trigger Point Indicator (a small "T" riding on the displayed waveform) indicates the scope is triggered on the last line of field 2.

i. Continue to rotate the TRIGGER LEVEL control counterclockwise while performing the CHECK during the following part.

j. CHECK—That the readout indicates progressively lower line numbers are being displayed for field 2 and that eventually the readout indicates the highest line number of the previous field for the multi-field input is being displayed. For example, using an NTSC signal, the readout should indicate "TVF1 263".

k. CHECK—That the readout Trigger Point Indicator (small "T" riding on the displayed waveform) indicates the scope is triggered on the last line of field 2.

l. Set the A VIDEO COUPLING (SET VIDEO menu) to ALT.

m. Use the TRIGGER LEVEL control to set the readout to "TVFLD 1", indicating that the first lines of both fields are displayed.

n. CHECK—That the readout Trigger Point Indicator (a small "T" riding on the displayed waveform) indicates the scope is triggered on the first lines of both fields.

NOTE

By switching A VIDEO COUPLING (SET VIDEO menu) between FIELD 1, FIELD 2, and ALT, it is easier to see which line for which field the scope is triggered on for ALT VIDEO COUPLING.

o. Rotate the TRIGGER LEVEL control slightly counterclockwise while performing the CHECK during the following part.

p. CHECK—That the readout indicates the highest line number common to both fields for the multi-field input signal. For example, using an NTSC signal, the readout should indicate "TVFLD 262".

q. CHECK—That the readout Trigger Point Indicator (a small "T" riding on the displayed waveform) indicates the scope is triggered on the last line COMMON to both fields. See the *NOTE* following part m above.

r. Push the front-panel button labeled "MENU OFF/EXTENDED FUNCTIONS" twice to display the Extended Functions menu. Push VIDEO OPT in the menu. Set CNT BOTH!F1 to F1.

s. Select SET VIDEO and set to FIELD 1. Repeat parts d to g to check that the line count displayed in step e is "TVF1 1" (set in step d) and continues to "TVF2 525" in step g (set in step f).

r. Disconnect the test setup.

15. Verify Teksecure Erase Memory Function (For instruments serial numbered B011821 and above only; instruments B011820 and below do not have this function.)

CAUTION

PERFORMANCE OF THIS STEP (15) IS OPTIONAL. If performed, it will erase from sequencer memory the Initial Setup established and stored at the beginning of this procedure. Any other sequences, stored reference waveforms, and waveforms saved on screen will be irretrievably lost.

This step uses the front panel to verify that the Teksecure Erase Memory feature erases sequencer and reference memories, as well as any waveforms currently saved on screen. It also verifies that the current front-panel setup is changed to the default values normally established when an INIT front-panel is performed.

NOTE

In addition to this step, an audit procedure is orderable (call (503) 627-2400) that performs a more direct verification of the status of the internal memory blocks. It requires removal of the instrument's cabinet and uses an emulator to look at memory contents. If such verification is necessary, it is strongly recommended that it be performed by Tektronix service personnel only. In any case, any procedure requiring cabinet removal must be referred to qualified service personnel.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see Step i in "INITIAL SETUP" at the start of this procedure).

Select TRIGGER MODE		
Set:	AUTO	On
Select VERTICAL MODE		
Set:	CH2	Off
Set:	CH1 VOLTS/DIV	5 V
	A SEC/DIV	100 μs

b. Save CH 1 trace in REF memory 1: Position the CH 1 trace to the graticule line 3 divisions above center screen, then push SAVE to display the SAVEREF SOURCE menu. Now push CH1 in the menu and, when the menu changes, push REF1.

c. Reposition CH 1 trace and save in REF memory 2: Position the CH 1 trace to the graticule line 1 division above center screen. Now push CH1 and, when the menu changes, push REF2.

d. Reposition CH 1 trace and save in REF memory 3: Position the CH 1 trace to the graticule line 1 division below center screen. Now push CH 1 and, when the menu changes, push REF3.

e. Reposition CH 1 trace and save in REF memory 4: Position the CH 1 trace to the graticule line 3 divisions below center screen. Now push CH 1 and, when the menu changes, push REF4.

f. Reposition CH 1 trace and display REF memories 1-4: Push ACQUIRE and move the "live" CH 1 trace to the bottom of the graticule. Push DISPLAY REF, and then push REF1 through REF4 to display the saved CH 1 traces. Five traces should now be displayed.

g. Display Teksecure Erase Memory menu: Push the front-panel button labeled "MENU OFF/EXTENDED FUNCTIONS" twice to display the Extended Functions menu. Next, push SYSTEM and, when the menu changes, push PANEL. Now push the TEKSECURE ERASE MEMORY to display that menu.

h. Execute Teksecure Erase Memory: Push ERASE. The instrument screen will blank momentarily and then the message "RUNNING SELF TEST" will appear.

Failure of the SELF TEST that runs when Erase Memory is executed—even for reasons not related to internal RAM memory blocks—causes the Extended Diagnostics menu to be displayed, rather than the Teksecure Status menu. If this is *not* the case, continue this procedure at part i. If the Extended Diagnostics menu *is* displayed, do the following:

1. Push the MENU OFF/EXTENDED FUNCTIONS button once to force display of the Teksecure Status menu.

2. Perform part i and determine the Erase Memory status as instructed.

3. If status is determined ERASED, continue this procedure at part j; otherwise, perform part g again to access the Teksecure Erase Memory

menu, and push ERASE to execute another Erase Memory. Then, if the Erase Memory Status menu is not already displayed, push the MENU, OFF/EXTENDED FUNCTIONS button once to force the display of the Teksecure Status menu. Now perform part i, and, if the status is not ERASED, refer the instrument to qualified service personnel for repair.

NOTE

Even if the Erase Memory status is determined successfully, the failure that resulted in the SELF TEST failure should be serviced. After completing this procedure, run the Self Calibration procedure, followed by the Self Diagnostics procedure. (See Sections 5 and 6 of this manual or Appendix A of the Operators Manual for instructions on how to perform these procedures). If both are not successful, refer the instrument to qualified service personnel.

i. VERIFY—Internal memory status: Confirm that the message ERASED appears immediately following the TEKSECURE ERASE MEMORY STATUS caption, as well as after each of the captions for the individual blocks of RAM memory. If FAILED appears after any caption, perform parts g and h again to reexecute an Erase Memory. If status is still failed, this verification fails and the instrument should be referred to qualified service personnel for repair.

j. VERIFY—Front-panel and screen status: Confirm that CH 1 is set to 100 mV (was set to 5 V in part a) and that the A SEC/DIV is set to 1 ms (was set to 100 μs in part a). Confirm that the four traces that were saved in and displayed from REF memories 1-4 are no longer displayed, and that the "live" CH 1 trace is displayed at or near center screen.

k. VERIFY—Reference Memory status: Push DISPLAY REF. Confirm that the status "EMPTY" is displayed above the REF 1-4 labels in that menu. Now use the menu buttons to first display and then remove each REF memory. Confirm that each memory displays an invalid "waveform" that is, a horizontal line at center screen that is broken by (alternates with) full-screen fill areas.

l. VERIFY—Sequencer Memory Status: Push PRGM to display the AUTOSTEP SEQUENCER menu; then push RECALL to switch to the menu for recalling sequences. Confirm that the label FPNL (the label for the Initial Setup sequence), is no longer listed for recall. Further, confirm that no other sequences are listed for recall.

Confirmation of parts i through l constitutes a verification of the Teksecure Erase Memory feature.

ADJUSTMENT PROCEDURE

INTRODUCTION

IMPORTANT—PLEASE READ BEFORE USING THIS PROCEDURE

This procedure is used to return the instrument to conformance with its "Performance Requirements" as listed in the "Specification" (Section 1). It can also be used to optimize the performance of the instrument. As a general rule, these adjustments should be performed every 2000 hours of operation or once a year if used infrequently.

The Adjustment Procedure consists of three subsections. The first subsection is "Internal Adjustments." Step 1 of this subsection, "Display Adjustments," uses display test patterns generated internally by the instrument. Steps 2 through 6 require external generators to provide signals for the test displays. In all steps of the "Internal Adjustments" internal controls must be adjusted (cabinet removal is required). An internal jumper must also be pulled off to enable the menu choices for the Extended Calibration menu. This menu must be enabled to perform "Display Adjustments" as well as the Attenuators and Triggers adjustments called out in the "External Calibration" subsection of this procedure.

The second subsection is "Self Calibration." SELF CAL is a fully automatic procedure initiated by the user from the front panel. No external signals or internal adjustments are required, and beyond starting the procedure, no further action is needed for the user to do a SELF CAL. The instrument cabinet must be installed to obtain a proper SELF CAL, and the Self Calibration subsection must be done and passed before going on to the third subsection of the Adjustment Procedure.

Subsection three is "External Calibration." Here, the user inputs test signals for the Attenuator and Trigger calibration and initiates the semiautomatic routines that use those signals. The internal jumper disabling the Extended Calibration (EXT CAL) menu must be removed to enable the EXT CAL menu choices (as was necessary for the Display Adjustments in "Internal Adjustments" subsection). The instrument cabinet must be installed and the instrument operating at an ambient temperature between +20°C and +30°C for valid calibration of the Attenuators and Trigger circuits.

CALIBRATION SEQUENCE AND PARTIAL PROCEDURES

To completely calibrate this instrument, all steps of this procedure should be performed, completely and in sequence. Individual steps in either the Internal Adjustments or External Calibration subsections can be omitted if a complete calibration is not needed. Individual substeps (parts) in "Display Adjustments" (Internal Adjustments subsection) can be skipped by advancing to the next display.

While a Self Calibration must be performed before doing the External Adjustments, it can also be performed any time the instrument is installed in its cabinet, optimizing the instrument's performance for the existing environment. The internal jumper removed for performance of the Internal Adjustments and External Calibration does not affect Self Calibration.

WARM-UP TIME REQUIREMENTS

This oscilloscope requires adequate warm-up time in a 20°C to 30°C environment before performing the calibration routines and adjustments in this procedure. Calibration performed before the operating temperature has stabilized may cause an erroneous calibration. The adjustment procedure indicates the duration of the warm-up periods and the points in the procedure at which they should be allowed.

PRESERVATION OF INSTRUMENT CALIBRATION

Both the Internal Adjustments and External Calibration subsections require enabling the EXTENDED CALIBRATION menu. Since the internal calibration constants stored can be altered by the user if the EXTENDED CALIBRATION menu is enabled, this menu is disabled by the installation of an internal jumper. REINSTALLATION OF THE INTERNAL JUMPER TO PREVENT INADVERTENT ALTERING OF INTERNAL CALIBRATION CONSTANTS BY USERS IS RECOMMENDED. Performance of a Self Calibration only, without performance of either of the other two subsections, does not require the removal of the jumper or cabinet.

NOTE

The Extended Calibration menu can also be accessed via the GPIB (General Purpose Interface Bus). See "Extended Calibration" in Appendix A of the Operators Manual for further information.

INTERNAL ADJUSTMENTS

Equipment Required (See Table 4-1):

- Primary Leveled Sine-Wave Generator (Item 1)
- Secondary Leveled Sine-Wave Generator (Item 2)
- Calibration Generator (Item 3)
- Coaxial Cable (Item 10)
- Precision Coaxial Cable (Item 11)
- 50 Ω Termination (Item 12)
- 10X Attenuator (Item 13)
- 5X Attenuator (Item 14)
- Dual-Input Coupler (Item 18)
- Alignment Tool (Item 25)
- Normalizer (Item 26)
- Tunnel-Diode Pulser (Item 27)

1. Display Adjustments.

a. Remove the cabinet from the instrument (see "Removal and Replacement Procedure" in the "Maintenance" section of this manual). Remove jumper J156 from P156 on the Side Board (on right side of instrument near the front).

NOTE

Operation (for more than a few minutes) of the scope without its cabinet installed requires that cooling be provided for the components on the Main board. Use a small fan to direct air across the finned heatsinks on that board. The fan used should have the same airflow capability as the fan used in the scope. The CFM (cubic feet per minute) specification for the instrument's fan is 35 CFM at 0 H_20 (essentially, open air). Do NOT remove the fan from the scope for use in cooling the Main board, as critical components in other sections of the instrument may overheat.

b. Connect the instrument to a suitable power source and power it ON. Allow a 10 minute warm up before performing the rest of this subsection.

c. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the EXT FUNCT Functions menu.

d. Press the menu button labeled CAL/DIAG (menu will change).

e. Press the menu button labeled EXT CAL to display the EXT CAL menu.

f. Press the menu button labeled ADJUSTS (Display 1 will appear).

g. ADJUST—The ASTIG and FOCUS front panel controls for best definition of the displayed dot.

h. Press any menu button to advance to Display 2.

NOTE

All adjustment controls associated with Displays 2 and 3 that are not designated front panel controls are located between the fan and the high-voltage shield on the left side board of the instrument.

i. ADJUST—R100 (Grid Bias control) as necessary to display two dots. Continue to adjust R100 just until one dot disappears, leaving the other dot displayed.

j. Press any menu button to advance to Display 3.

k. ADJUST—The ASTIG and FOCUS front panel controls and R300 (Edge Focus control) for most uniform focus over the entire displayed pattern.

l. ADJUST—The TRACE ROTATION front panel control to align the horizontal lines of the displayed pattern parallel to the horizontal graticule lines.

m. ADJUST—R305 (the Y-AXIS control) to align the vertical lines of the displayed pattern parallel to the vertical graticule lines.

n. REPEAT—Parts l and m to obtain best overall alignment.

o. ADJUST—R200 (Geometry control) for the least curvature overall of the display lines at the vertical and horizontal edges of the crt screen.

p. ADJUST—R300 (Edge Focus control) for best focus along the edges of the crt screen.

q. Set the INTENSITY control (front panel) for maximum brightness of the display. ADJUST—R400 (Hi-Drive Focus) for best overall focus of the displayed pattern.

r. Return the INTENSITY control to approximately the same setting in effect prior to part p and repeat parts p and q for best focus compromise between the two intensity settings.

s. Press any menu button to advance to Display 4. Note that all adjustment controls associated with this display are located on the top circuit board near the rear of the instrument (see Figure 5-1).

t. ADJUST—R583 (Vertical Spot-wobble control) and R584 (Horizontal Spot-wobble control) for maximum overall definition of the displayed dot pattern (only one dot visible at each graticule line intersection where a dot is displayed).

NOTE

When the Spot-wobble compensation is badly out of adjustment, three dots will be visible at each of the 33 dot locations. ADJUST—R583 or R584 to align the dots in either a vertically or horizontally oriented line, then use the other control to adjust for only one dot at each dot location (all three dots superimposed).

u. Press any menu button to advance to Display 5. Note that all adjustment controls associated with this display are located on the top circuit board near the rear of the instrument (see Figure 5-1).

NOTE

The display generated by performing part s is composed of a "rectangle" of dots, a small "cross" of 5 dots, and a large "cross" of 2 vectors. Calibration for this display consists of aligning the small cross to the large one (parts v and w), then aligning both crosses to the center graticule lines (parts x and y), and finally, adjusting the horizontal sides of the rectangle for 6 divisions of separation and the vertical sides for 8 divisions of separation (parts z and aa). See Figure 5-2 (a and b).

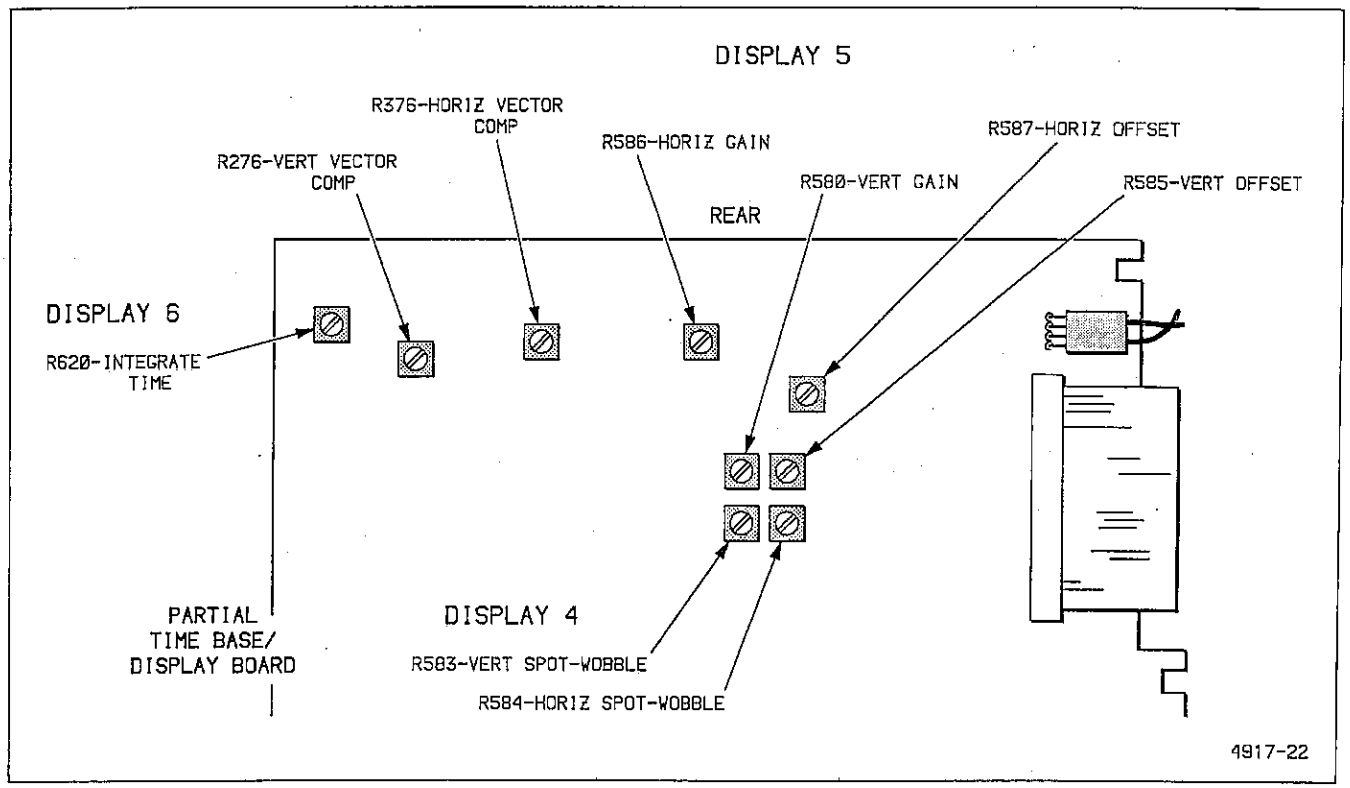
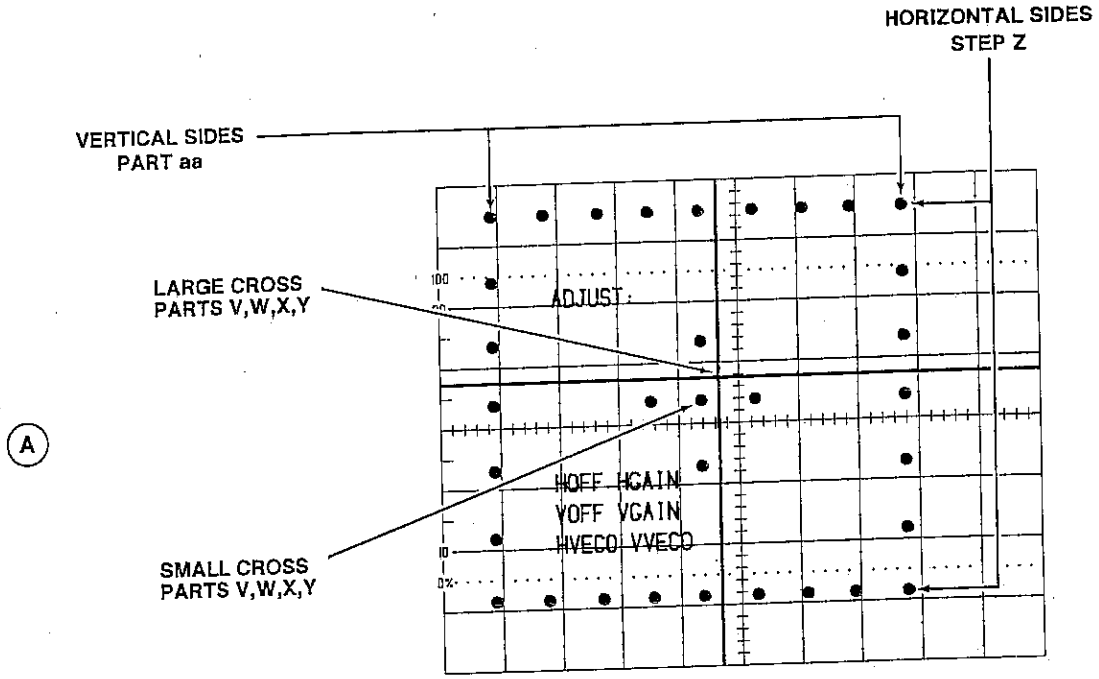
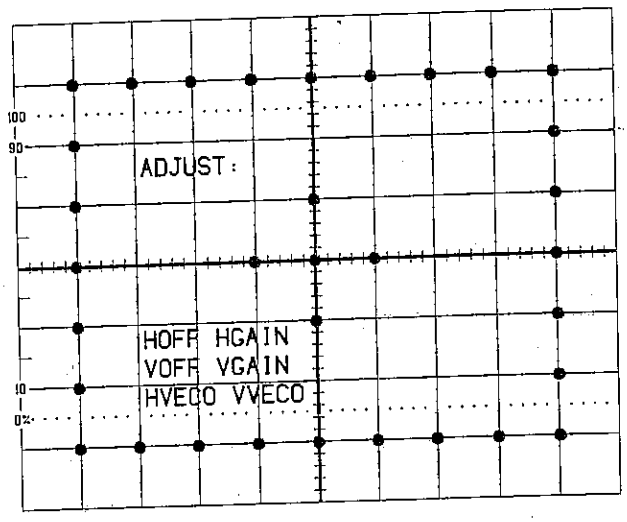


Figure 5-1. Adjustment locations for Displays 4 through 6.



A

Typical display (No. 5) needing adjustment. Arrows designate display components and procedure steps affecting those components.



B

Typical display (No. 5) when horizontal and vertical offsets, gains and vector compensations are correctly adjusted.

4917-16

Figure 5-2 (a and b). Display 5—Vertical and Horizontal Gain, Offset, and Vector Compensation adjustments pattern.

v. ADJUST—R276 (Vertical Vector Compensation control) to align the 3 vertically oriented dots of the small cross pattern to the vertical vector of the large cross pattern.

w. ADJUST—R376 (Horizontal Vector Compensation control) to align the 3 horizontally oriented dots of the small cross pattern to the horizontal vector of the large cross pattern.

x. ADJUST—R585 (Vertical Offset control) to precisely align the horizontal vector of the displayed pattern to the center horizontal graticule line.

y. ADJUST—R587 (Horizontal Offset control) to precisely align the vertical vector of the displayed pattern to the center vertical graticule line.

z. ADJUST—R580 (Vertical Gain control) to space the horizontal sides of the rectangle exactly 6 divisions apart.

aa. ADJUST—R586 (Horizontal Gain control) to space the vertical sides of the rectangle exactly 8 divisions apart.

ab. Press any menu button to advance to Display 6. Note that the adjustment control associated with this display is located on the top circuit board near the left rear corner of the instrument (see Figure 5-1).

ac. ADJUST—R620 (Integrator Time control) for best front corner (minimum roll-up or roll-off) of the high-frequency (filled) portion of the display. See Figure 5-3 for further detail.

ad. Push any menu button to exit display 6.

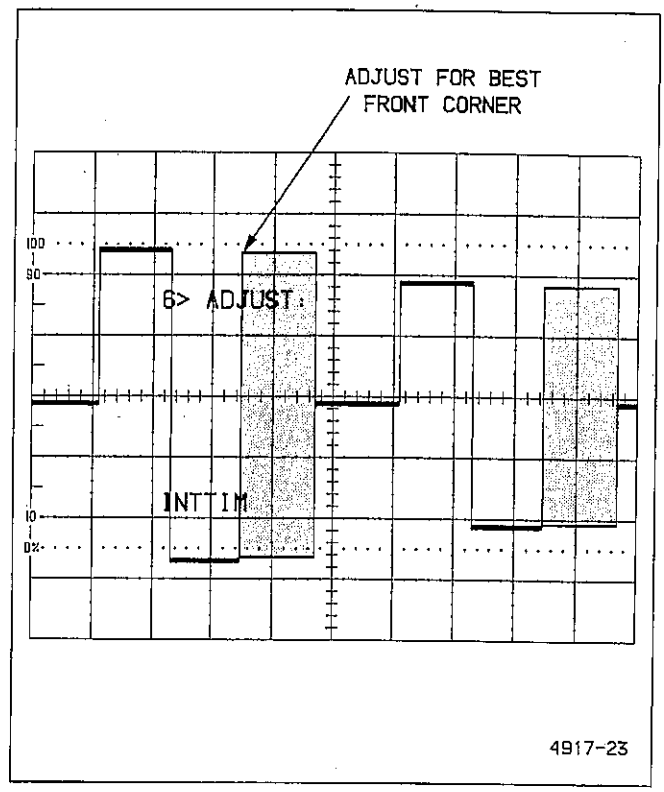


Figure 5-3. Display 6—Integrator Time adjustment pattern.

2. CCD Clocks Adjustment.

a. **Determine if CCD clocks need adjustment:**

- If doing this adjustment procedure after a repair that required replacing either or both CCD's (U450 and U350 on schematic diagram 10) or Peak Detectors (U440 and U340, also on diagram 10) or the CCD Phase Clock Generator (U470 on schematic diagram 11), the CCD clocks will need adjustment; skip to part b and continue this procedure.

- If doing this adjustment procedure as part of routine maintenance, or after a repair that did *not* require replacing the components just mentioned, do the following to determine if clock adjustment is adequate: perform part c to preset the instrument's front-panel controls (skip making the TRIGGER SOURCE setting). Next do part h and subparts 1-3 of part i to set up the instrument and the test generator for checking clock adjustments. Now, do part r, subparts 1-3. If part r is passed for both channels, CCD clock calibration is good; skip to step 3, "CH 1 and CH 2 Input Capacitance Adjustment". If part r is not passed, continue this procedure at part b.

b. **Preset clock adjustments:** Center all adjustment controls shown in Figure 5-4 so they are halfway between full clockwise and full counter-clockwise rotation.

c. **Initialize front-panel controls:** Push the SETUP PRGM front-panel button; then push the menu button labeled INIT. Push the TRIGGER SOURCE front-panel button and set LINE on (underline it) in the menu.

NOTE

This procedure for adjusting clocks assumes front-panel settings set by the PRGM INIT feature; change those settings only when directed to by this procedure.

d. **Preset Common-Mode counts:**

1. **Display GN-DAC counts:** Set CH 1 VOLTS/DIV control to 50 mV, and set the SEC/DIV to 500 ns. Rotate the CH 1 POSITION knob to move the display up off screen. Push MENU OFF/EXTENDED FUNCTIONS twice; then push the SPECIAL menu button, and, when the menu changes, push CCD ADJ. Now, push the ADJ T1 A2 menu button to display the A and T clock adjustment numbers (T1 A2 will be underlined).

2. **Display menu for adjusting CM counts:** Push MENU OFF/EXTENDED FUNCTIONS twice; then push the SPECIAL menu button, and, when the menu changes, push FORCE DAC. The menu for adjusting the CM counts should now be at the bottom of the screen, with the various CCD counts for the four CH 1 CCD sides and the message "TESTING CHANNEL 1" displayed above that menu. (See Figure 5-5.)

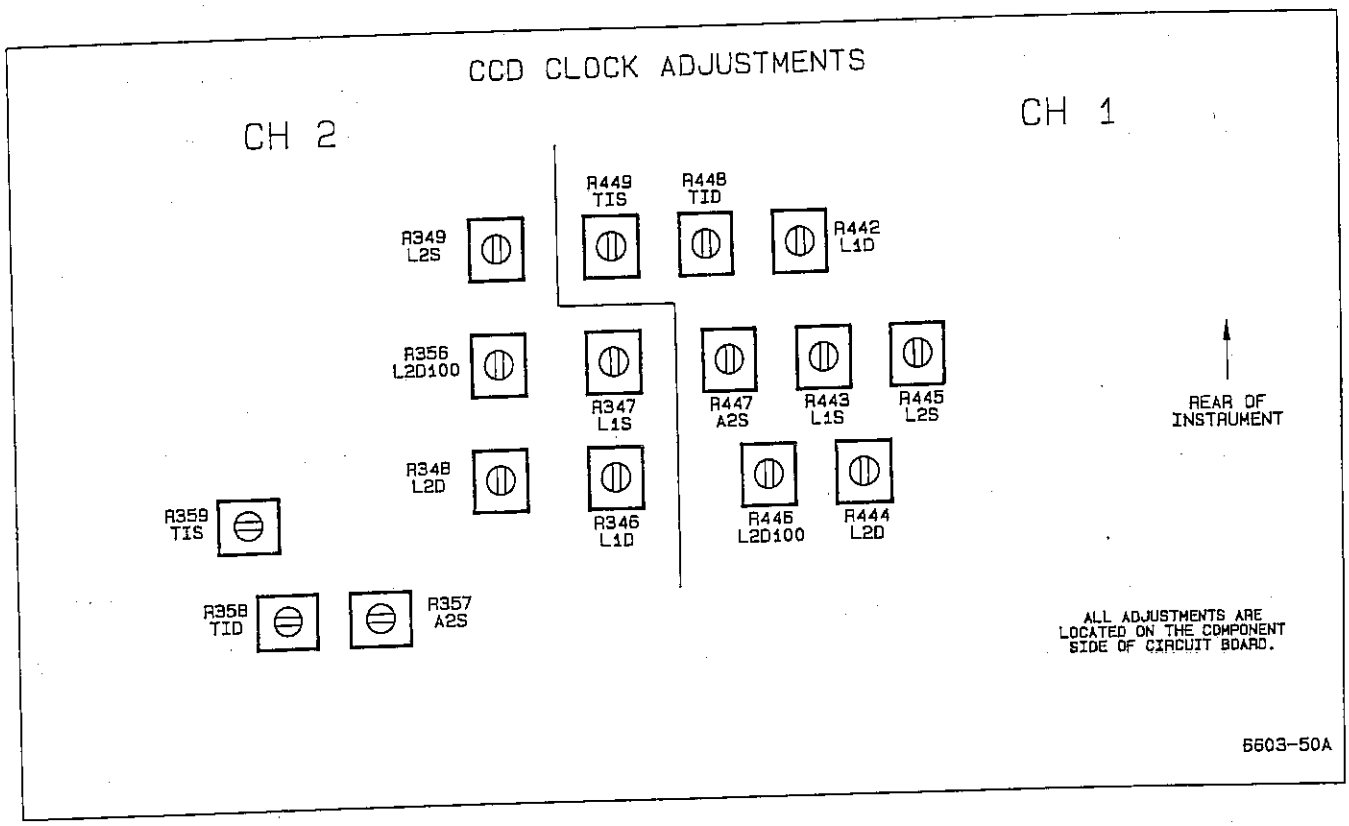


Figure 5-4 (SN B010250 & Above). CH 1 and CH 2 CCD Clock Adjustments (shown centered, as after doing part b).

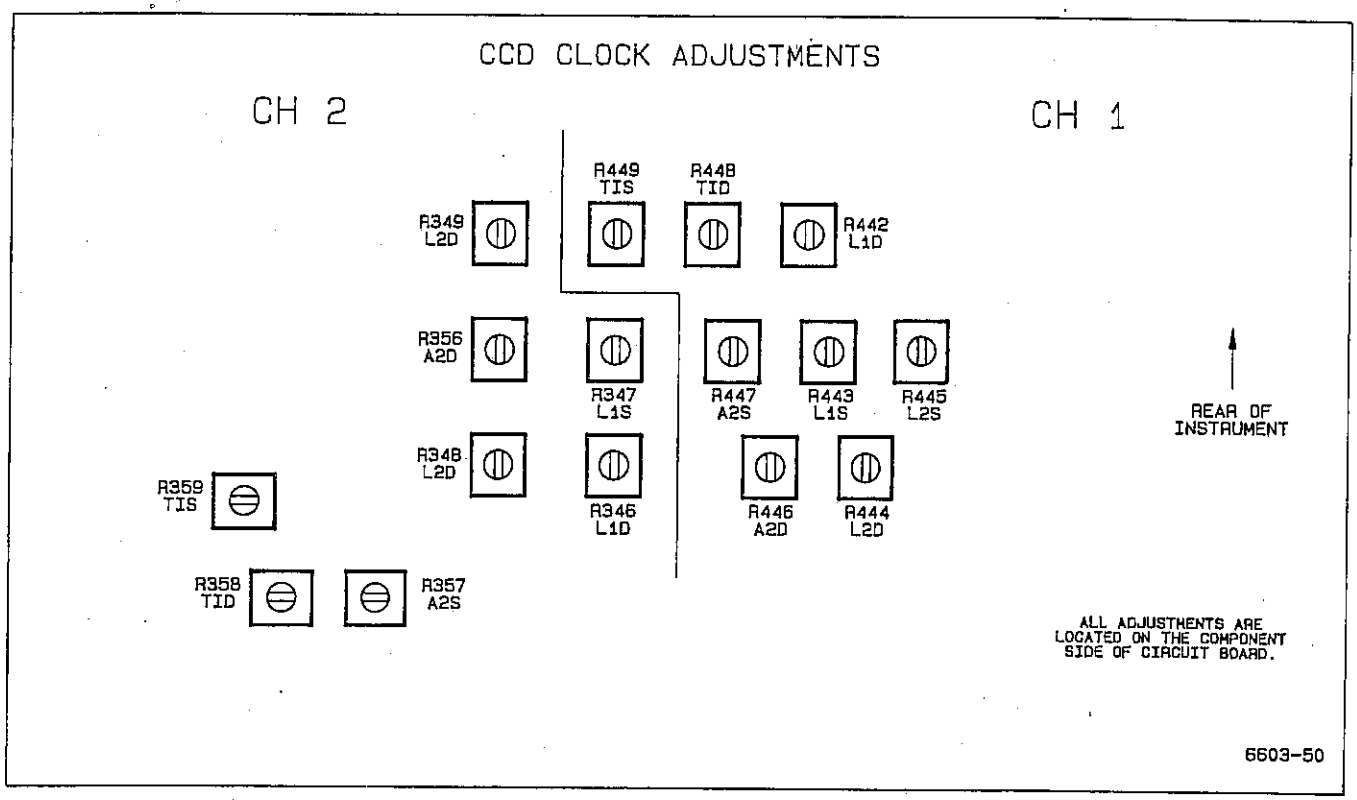


Figure 5-4 (SN B010249 & Below). CH 1 and CH 2 CCD Clock Adjustments (shown centered, as after doing part b).

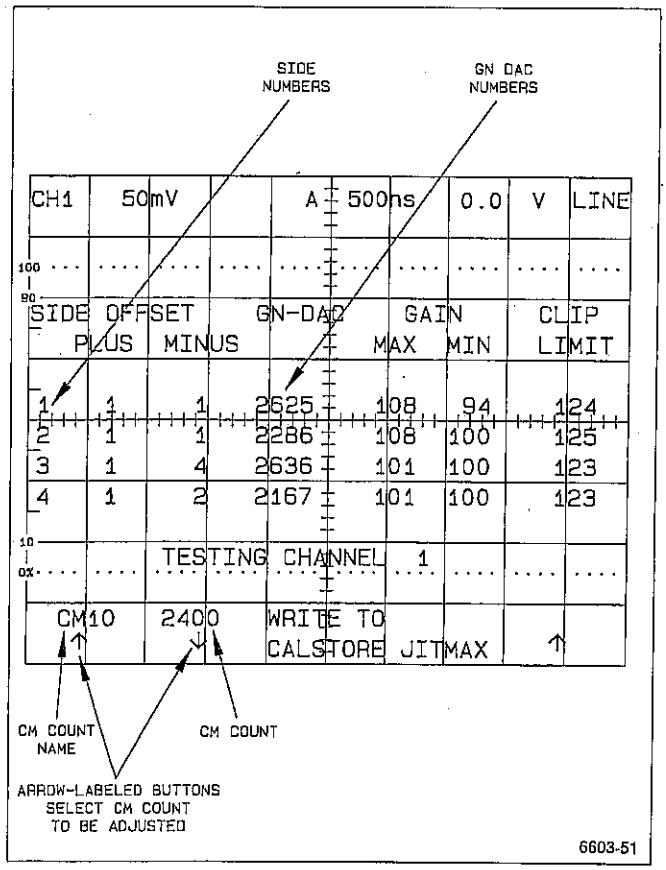


Figure 5-5. CCD counts display and CM adjustment menu.

3. **Set CM/GN-DAC counts, CH 1 sides 1 and 3, at 500 ns:** Repeatedly push the left-most menu button until the common-mode count for CM1O is displayed. Rotate the INTENSITY knob to set the CM1O count to 4095 (maximum count), and then do the following:

- If either GN-DAC counts for side 1 and 3 are below 500, refer the instrument to service personnel for repair.
- If the GN-DAC counts for both side 1 and side 3 are within 500-3200, push WRITE TO CAL STORE and skip to subpart 4.
- If the GN-DAC counts for either or both side 1 and 3 are above 3200 counts, reduce the CM1O count (CM1O stands for Common-Mode count, CH 1, Odd sides) *just enough to bring both counts to ⩽ 3200*, and then push WRITE TO CAL STORE. If CM1O must be reduced to below 1500 counts to bring both GN-DAC counts to within limits, or if both counts cannot be brought to within limits, refer the instrument to service personnel for repair.

4. **Set CM/GN-DAC counts, CH 1 side 2 and 4, at 500 ns:** Push the left-most menu button to move to CM1E (Common-Mode count, CH 1, Even sides); then rotate the INTENSITY knob to set this count to 4095. Now check, and set to within limits if necessary, the GN-DAC counts for sides 2 and 4 as was just done for sides 1 and 3 in subpart 3.

5. **Set CM/GN-DAC counts, CH 2 all sides, at 500 ns:** Rotate the CH 1 POSITION knob to return the CH 1 trace to center screen. Push VERTICAL MODE and set CH 2 on and CH 1 off in the menu. Set CH 2 VOLTS/DIV to 50 mV and rotate the CH 2 POSITION knob to move the CH 2 trace up off screen. Now, return to the CM counts menu: push MENU OFF/EXTENDED FUNCTIONS twice; then push SPECIAL; then push FORCE DAC. The menu for adjusting the CM counts should now be at the bottom of the screen, with the CCD counts for CH 2 CCD sides and the message "TESTING CHANNEL 2" displayed above that menu. Push the left-most menu button until CM20 appears; then repeat subparts 3 and 4, adjusting the CH 2 common-mode counts, CM2O instead of CM1O, and CM2E instead of CM1E.

6. **Turn off CCD counts display:** Vertically position CH 2 back to center screen. Next, push MENU OFF/EXTENDED FUNCTIONS twice; then push SPECIAL; then push CCD ADJ. Now, push the ADJ T1 A2 menu button to turn off the A and T clock adjustment numbers.

7. **Match CH 1 CM counts at 200 ns and 100 ns to 500 ns:** Push VERTICAL MODE and set CH 1 on and CH 2 off. Push MENU OFF/EXTENDED FUNCTIONS twice; then push the SPECIAL menu button, and, when the menu changes, push FORCE DAC. Note the CM1O and CM1E counts obtained in subpart 4. (Use the left- and right-most menu buttons to display CM1O and CM1E.) Now change the SEC/DIV setting to 200 ns, and use the INTENSITY control to set CM1O and CM1E to the values just noted. When finished, push WRITE TO CALSTORE, followed by the A HORIZONTAL MODE button. Change the SEC/DIV to 100 ns and match CM1O and CM2E to the 500 ns values also.

8. **Match CH 2 CM counts at 200 ns and 100 ns to 500 ns:** Push VERTICAL MODE and set CH 2 on and CH 1 off. Return the SEC/DIV to 500 ns. Repeat subpart 7 for CH 2, adjusting CM2O and CM2E, rather than CM1O and CM1E. Remember to push WRITE TO CALSTORE followed by A HORIZONTAL MODE after each CM adjustment.

e. **Do a SELF CAL and verify initial CCD gain:** Skip to, and perform, the procedure found under SELF CALIBRATION in this section. (At this stage of instrument adjustment, SELF CALIBRATION may take several minutes to run rather than the 10 seconds mentioned in the SELF CAL procedure.) If instrument passes the SELF CAL (see NOTE in SELF CAL procedure), skip to part f of this procedure and continue. If, after redoing a SELF CAL as directed in parts e and f of the SELF CAL procedure, any test level except level 7000 has FAIL status, quit this procedure and refer the instrument to service personnel.

If only test level 7000 failed, verify that CCD gain test 7210- 30 passed: repeatedly push the down-arrow menu button to move down the underline pointer at test level 0000 until it is under test level 7000. Push RUN/SEL, and when the menu changes, use the down-arrow button to underline 7200. Push RUN/SEL. Test levels 7210, 7220, and 7230 should all have PASS status (ignore 7240 and 7250); if so, push MENU OFF/EXTENDED FUNCTIONS to remove diagnostic menu and continue with subpart f; if not, quit this procedure and refer the instrument to qualified service personnel for repair.

f. **Check CH 2 and CH 1 LF-linearity and position-effect, and fine-adjust CM counts:**

1. **Set up instrument for check:** Set A SEC/DIV to 50 μs. Next, push COUPLING/INVERT and set 50 Ω ON!OFF to ON for both CH 1 and CH 2. Push ACQUIRE and set REPET ON!OFF to ON. Push TRIGGER SOURCE and set to VERT in the menu. Connect the + FAST RISE output of a Calibration Generator to the CH 2 input connector via a 50-Ω cable. Set the generator output for a 1 ms period and for exactly 2 vertical divisions (discount trace width) of amplitude. Vertically center the display.

2. **Make linearity check:** Rotate the CH 2 POSITION knob to align the bottom of the waveform to the horizontal graticule mark 2.5 divisions above the center horizontal graticule line (the top of the waveform will be off screen). Now push SAVE, vertically reposition the waveform to center screen, and check that the amplitude of the saved waveform is between 1.9 and 2.1 divisions. Push ACQUIRE and repeat the linearity check, this time aligning the *top* of the waveform to the mark 2.5 divisions below the center horizontal graticule line before pushing SAVE. Push ACQUIRE when finished.

3. **Make position-effect check:** Set SEC/DIV to 5 ns. Adjust the amplitude of the calibration generator for 5 divisions, vertically center the pulse, and

horizontally align its rising edge to center screen. Position the top of the waveform to 3.5 divisions below center graticule. Push ACQUIRE and set ENVELOPE to CONTinuous. Check that the vertical width of the trace between 5 ns and 15 ns after the step transition is less than 0.4 division. (Push MENU OFF/EXTENDED FUNCTIONS to turn off menu so the waveform can be easily seen.) Set A SEC/DIV to 500 ns. Push ACQUIRE and set back to NORMAL.

4. **Fine-adjust CM counts:** If both LF-linearity checks in subpart 2, as well as the position-effect check in subpart 3, were passed, skip to subpart 5. If either of the LF-linearity checks *and* the position-effect check failed, refer the instrument to qualified service personnel for repair. Otherwise, display the menu for adjusting the CM counts: Push MENU OFF/EXTENDED FUNCTIONS twice; then SPECIAL; then push FORCE DAC. Then, do the following:

- If either of the LF-linearity checks failed but the position-effect check passed, rotate the INTENSITY control to reduce CM2E by about 150 counts; then push WRITE TO CALSTORE; then push the A HORIZONTAL MODE front-panel button. Next, push the downward arrow menu button to display CM2O and reduce it by about 150 counts also; then push WRITE TO CALSTORE, followed by the A HORIZONTAL MODE button.

- If only position-effect check failed, repeat CM2E/CM2O adjustments as just described for the LF-linearity check failure except increase, rather than reduce, CM2E and CM2O by about 150 counts.

If you had to reduce/increase the CM counts, change the SEC/DIV setting to 200 ns and set CM2O and CM2E to the new values just set for the 500 ns setting. Switch to 100 ns and repeat. (Use the two left-most menu buttons to select between CM2O and CM2E; remember to always push WRITE TO CALSTORE, followed by the A HORIZONTAL MODE button after adjusting any CM count.) When finished, return the SEC/DIV setting to 50 μs and repeat subparts 2, 3, and 4 until the LF-linearity and position-effect checks pass or until CM count is below 1500. (Always match the CM counts at 200 and 100 ns when they are changed at 500 ns.) If any CM count must be reduced below 1500, the instrument should be referred to qualified service personnel for repair.

5. **GN-DAC counts check:** SEC/DIV should be set to 500 ns. Push MENU OFF/EXTENDED FUNCTIONS twice; then SPECIAL; then CCD ADJ. Push ADJ TI A2 to display the GN-DAC counts. ("TESTING CHANNEL 2" should be displayed.) Check that the GN-DAC counts for all four sides (1-4) are within 1000-3200. If one or more GN-DAC counts are outside this range, change test-selectable resistors R690 and R881 (located on Time Base board) to one of the three pairs of values given in Table 5-1. *Resistors must be changed as a pair.* If the out-of-limit GN-DAC counts are greater than 3200, increase R690 and R881 to next higher pair of values listed; if the GN-DAC counts are less than 1000, decrease the resistors to the next lower pair of values. Recheck GN-DAC counts and increase/decrease resistors to the next pair in table as required. If GN-DAC counts cannot be brought to within limits with values pairs given in Table 5-1, refer instrument to qualified service personnel for repair.

Table 5-1
Test Selectable Resistor Values
(R690 and R881)

R690	PART NUMBER	R881	PART NUMBER
100 Ω	321-0097-00	301 Ω	321-0143-00
107 Ω	321-0100-00	348 Ω	321-0149-00
110 Ω	321-0101-00	374 Ω	321-0152-00

6. **Check LF-linearity and position effect, and fine-adjust CM counts for CH 1:** Push the ADJ TI A2 menu button to turn off the GN-DAC counts display. Set the SEC/DIV to 50 μs. Move the 50-Ω cable at CH 2 to the CH 1 input connector. Push VERTICAL MODE, set CH 2 off and CH 1 on in the menu. Adjust the generator for exactly 2 vertical divisions (discount trace width) amplitude, vertically centered on screen. Now do subparts 2-5, using CH 1 controls instead of CH 2 controls and adjusting CM1O/CM1E where CM2O/CM2E are indicated. ("TESTING CHANNEL 1" will be displayed when subpart 5 is performed.) Any time R609 and R881 must be changed to bring either channel's GN-DAC counts within limits, subpart 5 must be reperformed for the other channel. If the resistors must be changed to a higher pair of values for one channel, only to require a lower pair for the other channel, or if both channels cannot be brought to within the GN-DAC count limits, refer this instrument to qualified service personnel for repair.

7. **Remove setup:** Push ACQUIRE and set REPET ON|OFF to OFF. Disconnect the cable from the CH 1 input connector.

g. **Check for correct CCD operation:**

1. **Display GN-DAC counts:** Push MENU OFF/EXTENDED FUNCTIONS twice; then push SPECIAL; then push CCD ADJ. Now, push the ADJ T1 A2 menu button to display the A and T clock adjustment numbers (T1 A2 will be underlined). The various CCD counts for the four CH 1 CCD sides should be on screen, with the message "TESTING CHANNEL 1" displayed near the bottom of the screen.

2. **Verify CH 1 counts are within limits:** Set the SEC/DIV control to 500 ns. Verify that the various counts for each of sides 1-4 are within the limits listed below. If any count is outside the limit listed, refer the instrument to service personnel.

SIDE	OFFSET		GN-DAC		GAIN	CLIP
	PLUS	MINUS	MAX	MIN	LIMIT	
1-4	≤10	≤10	500-3500	≤115	≥80	≥100

3. **Verify CH 2 counts are within limits:** Push VERTICAL MODE and set CH 2 on and CH 1 off in the menu displayed (message will change to "TESTING CHANNEL 2"). Verify that the various counts for each of the CH 2 sides 1-4 are within the limits listed for subpart 2. If any count is outside the limit listed, refer the instrument to service personnel.

4. **Turn off display of GN-DAC counts:** Redo subpart 1, pushing ADJ T1 A2 menu button to remove the display (the underline below T1 A2 is also removed.)

h. **Prepare instrument for adjusting L, TI, and A clocks:**

1. **Turn off display vectors:** Push the front-panel button SELECT, and when the menu changes, push the menu button to set VECTORS ON¦OFF to OFF (OFF should be underlined).

2. **Set input coupling:** Push CH 1 COUPLING/INVERT and set 50 OHMS ON¦OFF to ON (the coupling mode should already be set to DC) in the menu displayed. Push CH 2 COUPLING/INVERT and set 50 OHMS ON¦OFF to ON in that menu.

For SN B010250 & Above

3. **Input test signal:** Connect the output of the secondary Leveled Sine-wave Generator (Item 2) to the CH 1 and CH 2 input connectors via a precision 50-Ω BNC cable and a dual-input coupler.

For SN B010249 & Below

3. **Input test signal:** Connect the output of the primary Leveled Sine-wave Generator (Item 1) to the CH 1 and CH 2 input connectors via a precision 50-Ω BNC cable and a dual-input coupler.

i. **Set up to adjust the L clocks:**

1. **Set up Vertical mode, Trigger source, and acquisition rate:** Push the VERTICAL MODE front-panel button and turn CH 1 on in the menu displayed. Leave CH 1 on also; both channel's VOLTS/DIV setting should be 50 mV. Next, rotate the CH 2 POSITION knob to move the CH 2 trace up off screen. Push TRIGGER SOURCE, and then push the EXT menu button. When the menu changes, set A EXT SOURCE 1¦2 to 2 (underline the "2"). Set the SEC/DIV control to 200 ns.

NOTE

The following two subparts set up an "aliased" display on screen that is used in adjusting the L clocks. At the 200-ns per division setting specified in subpart 2, the acquisition rate will be lower than is required to properly display the 250-MHz sine wave specified in the same subpart. However, by slightly varying the generator output frequency as needed, an "aliased" display is created. The aliased sine wave appears as if it is untriggered and as if its frequency is much lower than the 250-MHz sine wave output by the generator. Use a generator with a highly stable frequency output, such as the TEKTRONIX SG 503.

For SN B010250 & Above

2. **Set up test signal:** Set the generator output level for about a 6-division display at a frequency of 6 MHz, then change the output frequency to 250 MHz. Readjust for a 6 divisions amplitude if necessary, and vertically center the display.

For SN B010249 & Below

2. **Set up test signal:** Set the generator output level for about a 6-division display at a frequency of 1 MHz, then change the output frequency to 250 MHz. Readjust for a 6 divisions amplitude if necessary, and vertically center the display.

3. **Alias display:** Vary the generator output frequency slightly (if required) until only one or two cycles of the untriggered sine wave are displayed (about ±100 kHz).

At this point, the display should appear similar to Figure 5-6 (except "live", not "frozen"); although offset (spacing) between the sides varies from instrument to instrument. Since the instrument is set up to auto-level trigger but given no trigger signal (EXT source), it freezes the display on screen about once every second. This makes it easier to see the results when making a clock adjustment.

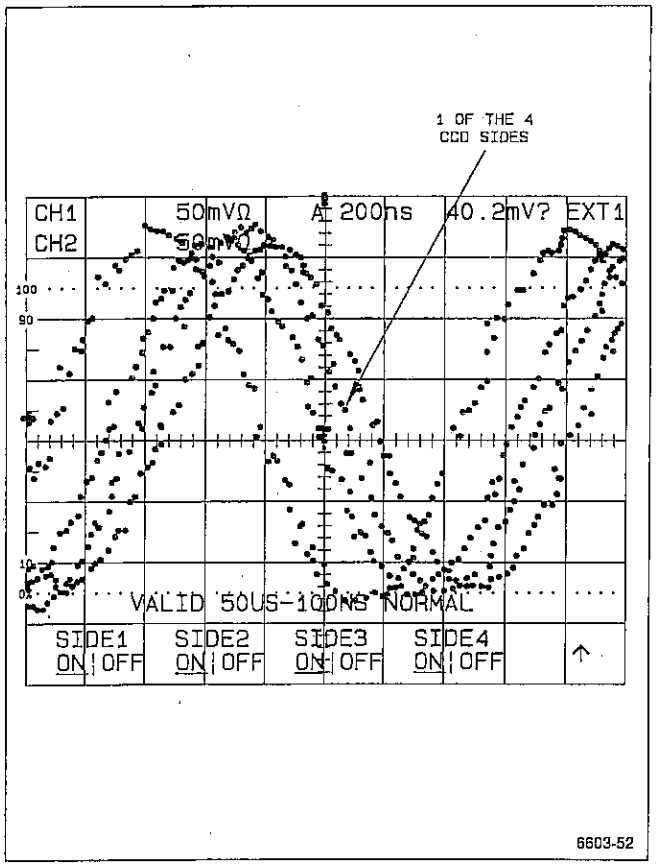


Figure 5-6. CCD sides 1-4 for CH 1 before L-clock adjustment. Note menu shows all sides are ON.

4. **Display CCD sides menu:** Push the MENU OFF/EXTENDED FUNCTIONS button twice to return to the Extended Functions menu; push SPECIAL and, when the menu changes, push CCD sides.

5. **Check/match coarse frequency response between channels:** Set sides 2, 3, and 4 off in the menu, leaving only side 1 on (underlined sides are on). Rotate the CH 2 POSITION knob to move the CH 2 display back on screen. Check that the difference between the amplitudes of the CH 1 and CH 2 displays is no more than 1 division. If mismatched by more than 1 division, adjust R436, C456, and R525 for CH 1 and R263, C257, and R410 for CH 2 until the amplitudes match. (The CH 1 adjustments are located near the front of the instrument on the Main board between the CH 1 Preamp IC, U420, and the shaft to the POWER ON OFF switch; the CH 2 adjustments are located between the CH 1 Preamp IC, U420 and the CH 2 Preamp IC, U320.) Position the CH 2 display off screen and turn back on all four sides when finished.

For SN B010250 & Above

NOTE

When a procedure part or subpart requires an adjustment, pay particular attention to whether CH 1 or CH 2 is to be adjusted. Both CH 1 and CH 2 have an LIS adjustment, an A2S adjustment, etc., so be sure you are setting the adjustment for the channel specified by the part; be sure *you are not setting the equivalent adjustment for the alternate channel. Use Figure 5-4 to locate the adjustments.*

For SN B010249 & Below

NOTE

When a procedure part or subpart requires an adjustment, pay particular attention to whether CH 1 or CH 2 is to be adjusted. Both CH 1 and CH 2 have an LIS adjustment, an A2D adjustment, etc., so be sure you are setting the adjustment for the channel specified by the part; be sure *you are not setting the equivalent adjustment for the alternate channel. Use Figure 5-4 to locate the adjustments.*

j. **Align the odd-numbered CH 1 CCD sides:** Set SIDE 2 and SIDE 4 to OFF in the menu. Set the CH 1 L1S adjustment for the best alignment of the two sides displayed (sides 1 and 3). Push A HORIZONTAL MODE, and readjust if necessary.

"Best Alignment" occurs when both sides are merged into a single side containing twice as many dots or samples. Figure 5-7 (a and b) shows typical "before and after" displays for adjustment of any two CCD sides; here, sides

1 and 3 for CH 1. When setting the L clocks to align any two given sides, set for equal alignment between the rising and falling portions of the sine wave; expect some mismatch of alignment between the peaks of the sides.

NOTE

Pushing A HORIZONTAL MODE causes the instrument to make firmware corrections based on the new adjustment just made for the L clock. These corrections may change the alignment slightly; in subparts j-n, repeatedly alternate between making the adjustment and pushing A MODE until no change is noted when the button is pushed.

k. **Align the even-numbered CH 1 CCD sides:** Set SIDE 2 and SIDE 4 back on, and set SIDE 1 and SIDE 3 to OFF. Set the CH 1 L2S adjustment for the best alignment of the two sides displayed. Push A HORIZONTAL MODE when finished.

l. **Align CH 2 even sides and odd sides:** Rotate the VERTICAL POSITION knobs to position the CH 1 display up off screen and the CH 2 back on screen. Repeat parts j and k, using the CH 2 L-clock adjustments to align the CH 2 CCD sides. *Be sure to adjust the CH 2 L1S and L2S adjustments and not the equivalent CH 1 L-clock adjustments that were just set.* See Figure 5-4 for adjustment locations.

m. **Align CH 1 sides to CH 2 sides:** Turn on SIDE 2 and turn all remaining sides off. Rotate the CH 1 POSITION knob to return CH 1 on screen positioned so that its ground reference indicator (a small "+" at the left edge of the screen) is on the center horizontal graticule line. Use the CH 2 POSITION knob to superimpose its ground reference indicator on CH 1's. Now, adjust CH 1 L2D for best alignment of the CH 1 and CH 2 sides. You may adjust CH 2 L2D if good alignment is not achieved. (If such is the case, alternate between the CH 1 and CH 2 L1D adjustments until best alignment is achieved.) Remember to push A HORIZONTAL MODE after making each adjustment.

n. **Align an even CH 1 CCD side to an odd:** Set SIDE 1 and SIDE 2 on and all remaining sides OFF. Position the CH 2 display up off screen. Now, adjust CH 1 L1D for best alignment of sides. Push A HORIZONTAL MODE.

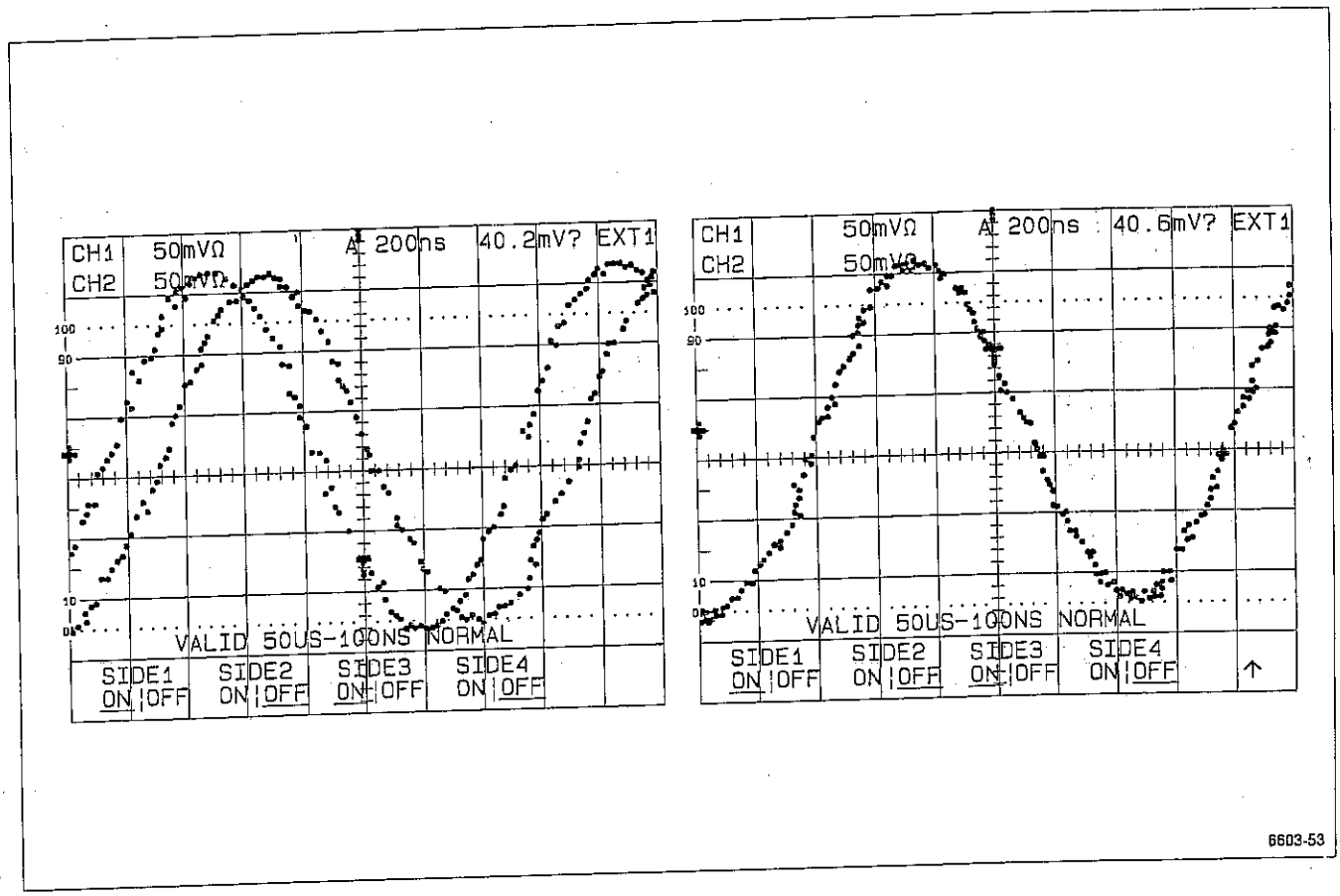


Figure 5-7 (a and b). Sides 1 and 3 before adjustment of L1S and after. Similar results should be obtained when adjusting any pair of sides with the L-clocks adjustments. (Best alignment that can be achieved varies from instrument to instrument.)

o. **Align an even CH 2 CCD side to an odd:** Position CH 1 up off screen and CH 2 on. Adjust the CH 2 L1D for best alignment of SIDE 1 and SIDE 2. Push A HORIZONTAL MODE.

p. **Check CH 1 and CH 2 L-clock adjustment:** Position both channels back on screen, and turn on all four CCD sides. Verify that each channel displays good alignment of its four sides. Repeat parts j through o as necessary to fine-tune the alignment.

q. **Adjust the A and T clocks:**

For SN B010250 & Above

1. **Coarse adjust the CH 1 A and T clocks:** Vertically position the CH 2 display off screen. Look at Figure 5-8 and note the stray samples labeled there. If the CH 1 display has similar "stray samples"—samples obviously offset from the well-aligned samples—adjust the CH 1 A and T clocks to align these stray samples. Begin with TID and TIS, and if necessary you can adjust A2S. Push A HORIZONTAL MODE after making each adjustment, iterating between making the adjustment and pushing A MODE as was done for the L-clock adjustment.

For SN B010249 & Below

1. **Coarse adjust the CH 1 A and T clocks:** Vertically position the CH 2 display off screen. Look at Figure 5-8 and note the stray samples labeled there. If the CH 1 display has similar "stray samples"—samples obviously offset from the well-aligned samples—adjust the CH 1 A and T clocks to align these stray samples. Begin with TID and TIS, and if necessary you can adjust A2D and A2S. Push A HORIZONTAL MODE after making each adjustment, iterating between making the adjustment and pushing A MODE as was done for the L-clock adjustment.

2. **Coarse adjust the CH 2 A and T clocks:** Vertically position the CH 2 display on screen; position the CH 1 display off screen. Repeat subpart 1, but use the CH 2 A and T clock adjustments instead of those for CH 1. See Figure 5-4 for adjustment locations.

3. **Display the A and T clock-adjustment counts:** Set CH 1 on and CH 2 off in the VERTICAL MODE menu. Leave CH 1 vertically positioned off screen. Push the MENU OFF/EXTENDED FUNCTIONS button twice; then push SPECIAL; then push CCD ADJ. Now, push the ADJ T1 A2 menu button to display the A and T clock adjustment numbers (T1 A2 will be underlined).

NOTE

After coarse adjustment performed in subparts 1 and 2, the adjustments outlined in subparts 4 through 7 are often not needed. When performing these subparts, adjust only if the specified check is failed.

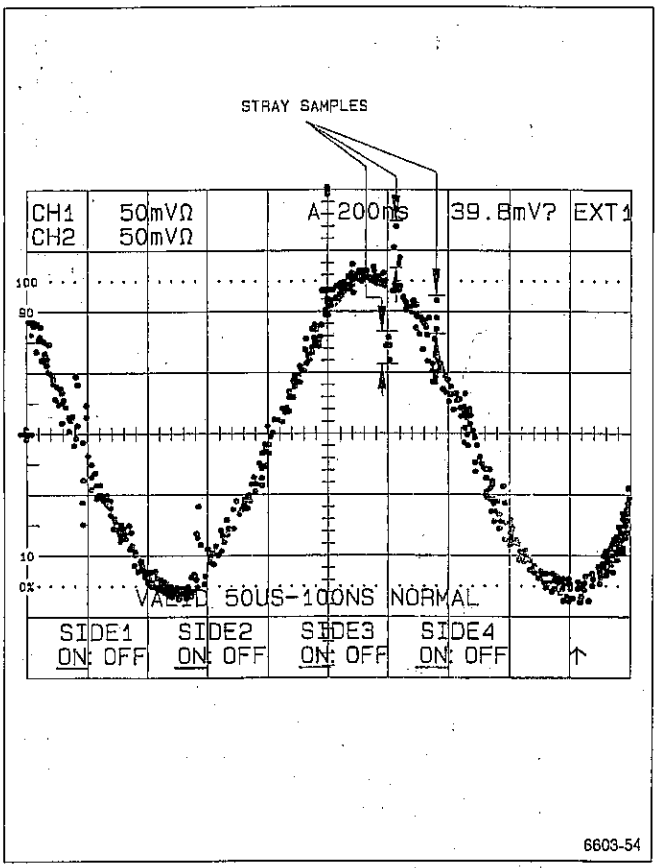


Figure 5-8. CH 1 with L-clocks correctly adjusted, but with stray samples.

For SN B010250 & Above

When making an adjustment after a failed check, start by adjusting TID and then TIS, continuing with A2S only if needed. Adjustment of these controls is best determined by trial: Start with TID and "rock" that adjustment back and forth to see if it improves the out-of-limit number(s), without moving the in-limit numbers out of limit. Continue with TIS and A2S as required; make the minimum number of adjustments that puts all the numbers within limits.

For SN B010249 & Below

When making an adjustment after a failed check, start by adjusting TID and then TIS, continuing with A2S and A2D only if needed. Adjustment of these controls is best determined by trial: Start with TID and "rock" that adjustment back and forth to see if it improves the out-of-limit number(s), without moving the in-limit numbers out of limit. Continue with TIS and the remaining two adjustments as required; make the minimum number of adjustments that puts all the numbers within limits.

For SN B010250 & Above

4. **Check CH 1 clocks at 100 ns and adjust if needed:** Set the SEC/DIV to 100 ns. *If required,* adjust (see NOTE below) the CH1 TIS, TID, and A2S adjustments so that all four sides (numbered 1-4 at extreme left) have GN-DAC counts within 700-3500, GAIN MIN counts greater than 92, and the CLIP LIMIT counts greater than 112 for *any* two sides and greater than 109 for the remaining two sides. (It doesn't matter which two sides are greater than 112 and which are greater than 109, just as long as at least two are greater than 112 and two are greater than 109. Also, all sides can be greater than 112.) See Figure 5-9.

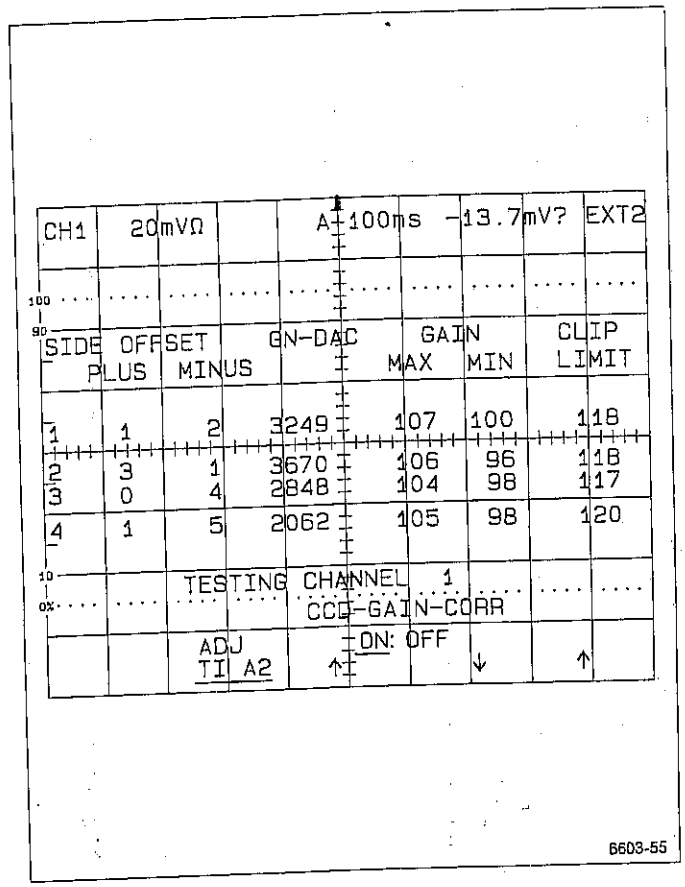


Figure 5-9. Display for adjusting CCD A and T clocks. Note this is the same display for presetting the CM counts, except no CM count adjustment menu is displayed.

For SN B010249 & Below

4. **Check CH 1 clocks at 100 ns and adjust if needed:** Set the SEC/DIV to 100 ns. *If required,* adjust (see NOTE below) the CH1 TIS, TID, A2D, and A2S adjustments so that all four sides (numbered 1-4 at extreme left) have GN-DAC counts within 700-3500, GAIN MIN counts greater than 92, and the CLIP LIMIT counts greater than 112 for *any* two sides and greater than 109 for the remaining two sides. (It doesn't matter which two sides are greater than 112 and which are greater than 109, just as long as at least two are greater than 112 and two are greater than 109. Also, all sides can be greater than 112.) See Figure 5-9.

5. **Check CH 1 clocks at 200 ns and adjust if needed:** Set the SEC/DIV to 200 ns. If required, adjust as for 100 ns setting, except two sides must be greater than 119 and the remaining sides greater than 115 (GN-DAC and CLIP LIMIT requirements are the same as for 100 ns). If adjustment is made, recheck at 100 ns when finished and readjust as necessary.

6. **Check/adjust CH 1 A and T clocks at 500 ns:** Set the SEC/DIV to 500 ns. If required, adjust as for the 100 and 200 ns settings, except two sides must be greater than 122 and the remaining sides greater than 119 (GN-DAC and CLIP LIMIT requirements are the same as for 100 ns). Recheck at 100 ns and 200 ns when finished and readjust as necessary.

For SN B010250 & Above

7. **Check/adjust CH 2 A and T clocks:** Push VERTICAL MODE and set CH 1 off and CH 2 on in the menu displayed. Use the CH 2 POSITION knob to move the CH 2 display up off screen. Now, repeat subparts 2-4 making the CH 2 TIS, TID, and A2S adjustments (only if needed) instead of the CH 1 adjustments (see Figure 5-4).

For SN B010249 & Below

7. **Check/adjust CH 2 A and T clocks:** Push VERTICAL MODE and set CH 1 off and CH 2 on in the menu displayed. Use the CH 2 POSITION knob to move the CH 2 display up off screen. Now, repeat subparts 2-4 making the CH 2 TIS, TID, A2D, and A2S adjustments (only if needed) instead of the CH 1 adjustments (see Figure 5-4).

8. **Turn off display for adjusting A and T clocks:** Set both CH 1 and CH 2 on in the VERTICAL MODE menu. Vertically position both CH 1 and CH 2 waveforms back on screen. Restore the CCD ADJ menu by pushing MENU OFF/EXTENDED FUNCTIONS twice; then SPECIAL; then CCD ADJ. Push ADJ T1 A2 menu button to turn off the display of the A and T clock adjustment numbers (underline is removed).

9. **Do a SELF CAL:** Skip to, and perform, the procedure found under SELF CALIBRATION in this section. (At this stage the instrument may take several minutes to run.) If the instrument passes the SELF CAL (see NOTE in SELF CAL procedure), skip to part r of this procedure and continue. If, after redoing a SELF CAL as directed in parts e and f of the SELF CAL procedure, any test level has FAIL status, quit this procedure and refer the instrument to qualified service personnel for repair.

r. **Check CH 1 and CH 2 A and T clocks' overall adjustment :**

1. **Set up for checking CCD side alignment:** The SEC/DIV control should be set to 200 ns. Adjust generator frequency to display about 2 cycles on screen.

2. **Verify good alignment of, and between, CH 1 and CH 2 waveforms:** Push SAVE and use the CH 1 and CH 2 POSITION controls to position the CH 1 and CH 2 for easy viewing. Check that the four sides of both the CH 1 and CH 2 waveforms are well-aligned and appear as single sine wave in each channel (see Figure 5-10). Now use the VERTICAL POSITION knobs to superimpose the CH 1 and CH 2 waveforms. Check that the CH 1 and CH 2 waveforms are well aligned; i. e., the superimposed sine waves should look like a "fatter" version of the CH 1 and CH 2 sine waves.

NOTE

Mainly check the falling and rising parts of the sine wave, rather than the peaks, since the amplitude may differ somewhat between channels as the instrument has not been completely adjusted.

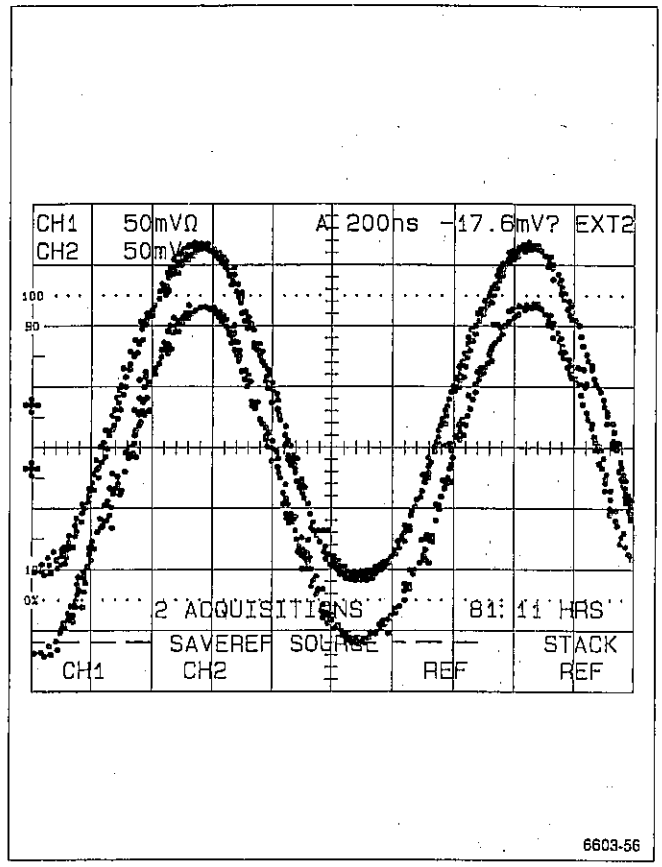


Figure 5-10. Typical CH 1 and CH 2 displays after clock adjustment.

3. **Check sample dispersion:** Now, push STORAGE ACQUIRE and vertically position the CH 1 and CH 2 display about 1 division apart. Adjust the frequency of the test generator for about a third of a cycle display in each channel. Push SAVE to capture a rising or falling portion of the waveform. (Watch the untriggered display until the desired portion is on screen and quickly push SAVE to capture; push ACQUIRE and repeat if unsuccessful.) Check to see that the dispersion of the samples on each section is no greater than one vertical division for each channel, and that there is no more than 1/2 division of difference between the two channels (see Figure 5-11).

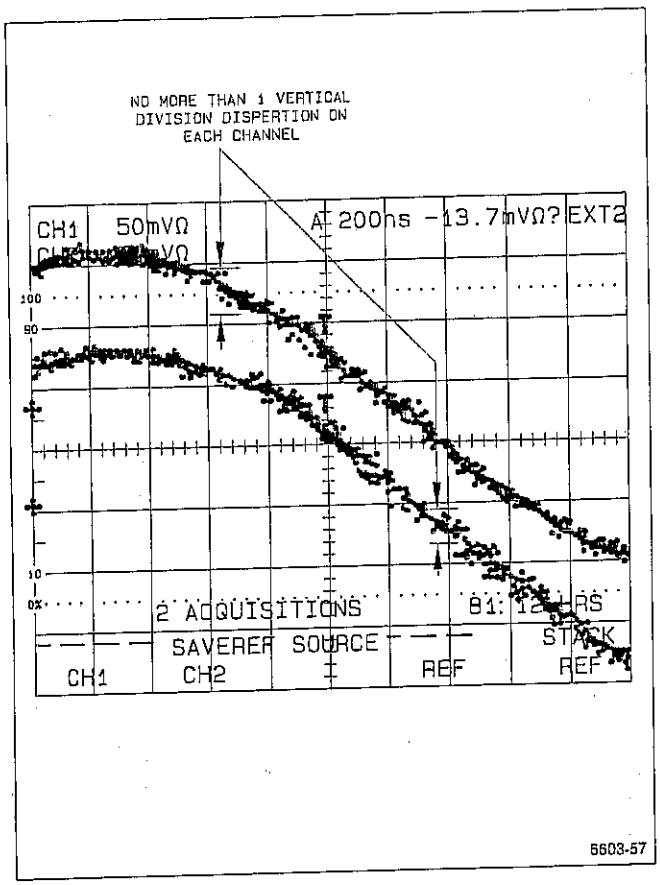


Figure 5-11. Checking sample dispersion.

4. **If either CH 1 or CH 2 fail the checks just performed, redo parts i-q to improve adjustment of L, A, and T clocks to meet checks.** (Push STORAGE ACQUIRE to return to a "live" display.)

For SN B010250 & Above (Step s and subparts only)

s. **Adjust the 100 ns L clocks:**

1. **Set up instrument:** Set the SEC/DIV to 100 ns. Vertically position the CH 2 display up off the screen.

2. **Set up test signal:** Set the generator output level for about a 4-division display at a frequency of 1 MHz, then change the output frequency to 500 MHz. Readjust for a 4 division amplitude if necessary, and vertically center the display.

3. **Alias display:** Vary the generator output frequency slightly (if required) until only one or two cycles of the untriggered sine wave are displayed (about ±100 KHz).

4. **Adjust CH 1 100 ns L clock:** Set the CH 1 L2D100 adjustment for the best alignment of all 4 sides (minimum sample dispersion). Push A HORIZONTAL MODE, and readjust if necessary. Continue to iterate until no change is noted when A HORIZONTAL MODE is pushed.

5. **Adjust CH 2 100 ns L clock:** Vertically position the CH 1 display up off screen, and position the CH 2 display back on screen. Set the CH 2 L2D100 adjustment for the best alignment of all 4 sides (minimum sample dispersion). Push A HORIZONTAL MODE, and readjust if necessary. Continue to iterate until no change is noted when A HORIZONTAL MODE is pushed.

t. Disconnect test setup.

3. CH 1 and CH 2 Input Capacitance Adjustment (C414 and C311).

a. If a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SETUP PRGM and press the menu button labeled INIT PANEL. Make the following changes to the front panel setup:

Set:	A SEC/DIV	100 μs

b. Connect the HIGH AMPLITUDE output of the Calibration Generator to the CH 1 input connectors via a precision 50 Ω BNC cable, a 50 Ω terminator, and an adjustable normalizer.

c. Set the generator output level for a 6 division display at a frequency of 1 kHz.

d. Set the normalizer for a square front corner over approximately the first 40 μs (0.4 division) of the positive portion of the waveform.

e. Change the CH 1 VOLTS/DIV control to 50 mV and adjust the generator amplitude for a 6 division display.

f. ADJUST—C414 (near the front edge of the Main board) for the same waveform front corner as noted in part d.

g. Repeat parts c through f until no change is observed in the waveform front corner between the 50 mV and 100 mV settings for the CH 1 VOLTS/DIV control.

h. Move the input signal to CH 2. Select VERTICAL MODE and set CH 2 on and CH 1 off.

i. Repeat parts c through g to adjust the CH 2 input capacitance, adjusting C311 in part f and using the CH 2 VOLTS/DIV control for parts e and g.

j. Disconnect the test setup.

4. Transient Response Adjustment.

a. **Set up to adjust transient response:**

1. **Initialize front panel:** Push the SETUP PRGM front-panel button; then push the menu button labeled INIT.

NOTE

Subpart 1 initializes the front-panel controls to known settings. Make only the changes outlined in the following procedure parts to avoid incorrect setups.

2. **Modify initial control settings:** Set CH 1 VOLTS/DIV to 20 mV and the SEC/DIV control to 5 μs. Push the CH 2 COUPLING/INVERT front-panel button and set 50 Ω ON:OFF to ON in the menu. Repeat for CH 1. Now, push STORAGE ACQUIRE and set REPET ON:OFF to ON in the menu.

3. **Set up test signal:** Connect the HI-AMPLitude output of a pulse generator to the CH 1 input through a 50-Ω precision cable, a tunnel-diode pulser, and a 2.5X attenuator. Set the generator's frequency to 100 kHz and the amplitude to maximum. Now, set the Trigger Level control of the TD Pulser to minimum (full counterclockwise rotation); then slowly rotate control clockwise just until a pulse five divisions in amplitude appears on screen. (Use the minimum Trigger Level setting that triggers the pulse.) Vertically center the display. Increase the SEC/DIV setting to 2 ns and push the INIT@50% front-panel button.

b. **Adjust CH 1 transient response:** Adjust R436, C456, and R525 for best front-corner. (These adjustments are located near the front of the instrument on the Main board between the CH 1 Preamp IC, U420, and the shaft to the POWER ON OFF switch.)

c. **Adjust CH 2 transient response:** Disconnect the test signal at the CH 1 input and move to the CH 2 input. Push VERTICAL MODE and set CH 2 on and CH 1 off. Set CH 2 VOLTS/DIV to 20 mV and vertically center the display as required. Now, adjust R263, C257, and R410 for best front-corner. (These adjustments are located near the front of the instrument on the Main board between the CH 1 Preamp IC, U420 and the CH 2 Preamp IC, U320.)

d. **Verify CH 2 and CH 1 bandwidth at 20 mV/division:**

1. **Set up the instrument for bandwidth verifications:** Change the SEC/DIV control to 5 ns. Disconnect the pulse generator output from the CH 2 input. Now, connect the output of the secondary Leveled-sine Wave Generator (Item 2) to the CH 2 input through the output head and a 10X attenuator. Set the test generator for a reference 6-division, 6-MHz signal display vertically centered on screen.

2. **Verify CH 2 bandwidth:** Switch the SEC/DIV control to 2 ns; then increase the test generator frequency until the amplitude decreases to 4.4 divisions on screen. The frequency should be greater than or equal to 310 MHz. Write down the frequency and the channel tested for use in the following subparts.

NOTE

If the frequency at 4.4 division is not greater than or equal to 310 MHz, readjust the transient response for the appropriate channel until the 310 MHz or greater bandwidth is obtained.

3. **Verify CH 1 bandwidth:** Return the SEC/DIV setting to 50 ns; push VERTICAL MODE and set CH 1 on and CH 2 off in the menu displayed. Move the signal from the CH 2 input to the CH 1 input, and set the test generator for a reference 6 division, 6-MHz signal, vertically centered on screen. Switch the SEC/DIV control to 5 ns; then increase the test generator frequency until the amplitude decreases to 4.4 divisions on screen. The frequency should be greater than or equal to 310 MHz (see NOTE for subpart 2). Write down the frequency and the channel tested for use in the following subparts.

e. **Match CH 1 bandwidth at remaining VOLT/DIV settings:**

NOTE

The following subparts attempt to match each channel's frequency response for all other VOLTS/DIV settings to that for the 20 mV setting. In some cases, you may not be able to adjust the number of divisions specified in the subpart (either 3.7 or 4.4 divisions) at the frequency obtained for the 20-mV setting in part f; if this is the case, just adjust as close as possible and check that the number of divisions obtained is ≥ 4.4 (3.7 for subpart 3) up to 310 MHz.

1. **Display menu for matching bandwidth:** Push MENU OFF/EXTENDED FUNCTIONS twice; then push the SPECIAL menu button, and, when the menu changes, push FORCE DAC. Now, push the left-most menu button until TRN1 is displayed near the lower-left corner of the screen.

2. **Set up CH 1 for adjusting 1-V bandwidth:** Set the CH 1 VOLT/DIV to 1 V. Remove the 10X attenuator and connect the generator's leveling head directly to the CH 1 input. Return the SEC/DIV to 50 ns and set the generator for the 5 division, 6-MHz reference signal. Change the SEC/DIV setting to 2 ns and increase the generator frequency to that written down for subpart 3 of part d.

3. **Adjust the 1-V bandwidth:** Rotate the INTENSITY knob to increase or decrease the waveform's amplitude to set to 3.7 divisions. Push WRITE TO CALSTORE menu button when finished.

4. **Set up CH 1 for adjusting 100-mV bandwidth:** Set the CH 1 VOLT/DIV to 100 mV. Return the SEC/DIV to 50 ns and set the generator for the 6-division, 6-MHz reference signal. Change the SEC/DIV setting to 2 ns and increase the generator frequency to that written down for subpart 3 of part d.

5. **Adjust the 100-mV bandwidth:** Rotate the INTENSITY knob to increase or decrease the waveform's amplitude to set to 4.4 divisions. Push WRITE TO CALSTORE menu button when finished.

6. **Set up CH 1 and adjust the 50-mV bandwidth:** Install a 10X attenuator between the generator's leveling head and the CH 1 input, and set the CH 1 VOLT/DIV to 50 mV. Repeat subparts 4 and 5, using the 50 mV VOLTS/DIV setting instead of 100 mV.

7. **Adjust the 10 mV, 5 mV, and 2 mV bandwidth:** Install a 5X attenuator between the 10X attenuator and the CH 1 input. Perform subparts 4 and 5 for the 50-mV, 10-mV, 5-mV, and 2-mV settings to match the bandwidth for each of those settings. Remember to push WRITE TO CALSTORE after making the TRN1 adjustment at each VOLTS/DIV setting.

f. **Match CH 2 bandwidth remaining VOLTS/DIV settings:** Push VERTICAL MODE and set CH 2 on and CH 1 off. Move the test signal from the CH 1 input to the CH 2 input, removing both the 5X and 10X attenuators. Now repeat subparts 1-7 of part e, selecting and setting TRN2 instead of TRN1 in subpart 1, setting the generator to the frequency written down for subpart 2 of part d instead of for subpart 3, and setting the CH 2 VOLTS/DIV control instead of the CH 1 in subparts 2-7.

g. Disconnect the test setup and push MENU/OFF EXTENDED FUNCTIONS to exit the menu.

5. 100 MHz Bandwidth Limit Filter Adjustment (Non-TV Options Only).

a. If a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SETUP PRGM and press the menu button labeled INIT PANEL. Make the following changes to the front panel setup:

Set:	A SEC/DIV	50 ns
	CH 1 VOLTS/DIV	10 mV
Select BANDWIDTH		
Set:	50 MHz	On
Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON:OFF	ON
Select STORAGE ACQUIRE		
Set:	REPET ON:OFF	ON
	AVG	On (8)

b. Connect the positive-going, FAST RISE output of the Calibration Generator to the CH 1 input via a precision 50 Ω cable and a 10X attenuator.

c. Set the generator output level for a 5 division display at a frequency of 100 kHz.

d. ADJUST—R431 for as flat a response as possible. This potentiometer is located on the Main circuit board.

e. Move the test setup to the CH 2 input connector.

f. Select VERTICAL MODE and set CH 2 on and CH 1 off.

g. Set CH 2 VOLTS/DIV to 10 mv.

h. Repeat parts c and d, adjusting R233 for part d.

i. Disconnect the test setup.

6. 20 and 100 MHz Bandwidth Limit Filter Adjustment (TV-Option 05 Only)

a. If a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SETUP PRGM and press the menu button labeled INIT PANEL. Make the following changes to the front panel setup:

Set:	A SEC/DIV	50 ns
	CH 1 VOLTS/DIV	10 mV
Select BANDWIDTH		
Set:	20 MHz	On
Select CH 1 COUPLING/INVERT		
Set:	50 Ω ON/OFF	ON
Select STORAGE ACQUIRE		
Set:	REPET ON/OFF	ON
	AVG	On (8)

b. Connect the positive-going, FAST RISE output of the Calibration Generator to the CH 1 input via a precision 50 Ω cable and a 10X attenuator.

c. Set the generator output level for a 5 division display at a frequency of 100 kHz.

NOTE

Adjust the coils in the following parts so their slugs are out approximately the same amount.

d. ADJUST—L531 for as flat a response as possible. This coil is located on the Main circuit board.

e. Move the test setup to the CH 2 input connector.

f. Select VERTICAL MODE and set CH 2 on and CH 1 off.

g. Set the CH 2 VOLTS/DIV control to 10 mV.

h. Repeat parts c and d for CH 2, adjusting L431 for part d.

i. Set the A SEC/DIV control to 100 μs.

j. Connect the Leveled Sine-wave Generator output via a 50 Ω precision cable and two 10X attenuators to the CH 2 input connector.

k. Set the generator to produce a 50 kHz, 5 division display.

l. Increase the generator output to 5 MHz and set the SEC/DIV control to 500 ns.

m. Check that the display amplitude is between 4.80 and 5.05 divisions.

n. Select BANDWIDTH and set 100 MHz on. Set the A SEC/DIV control back to 50 ns.

o. Select VERTICAL MODE and set CH 1 on and CH 2 off.

p. Repeat parts b through h to adjust the 100 MHz bandwidth limit, adjusting R431 and R233 in part d (adjust R431 when adjusting for CH 1, R233 for CH 2). These resistors are located on the Main board.

q. Disconnect the test setup.

7. Video Input Gain Adjustment (TV-Option 05 Only)

NOTE

In part a, you will connect the ground lead of a X10 probe to pin 5 of J125 on the processor board. Be sure you are connecting to the correct pin. Pin 1 is marked with a square pad, and all odd-numbered pins are in the same row as pin 1. Pin 5 is the second pin up from pin 1.

a. First, power the scope off. Then, perform subparts b-f of part 3 of the Removal and Replacement procedure in Section 6 to access the processor board of the instrument. Connect a X10 probe to the CH 2 input; then connect the ground lead of that probe to pin 5 of J125 of the processor board and the probe tip to the cathode of CR502. (CR502 is immediately above Q504 on the processor board; see the Processor Board drawing in the Diagrams section to locate CR502.) Power the scope back on.

b. Set up the scope: if a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SETUP PRGM, and press the menu button labeled INIT PANEL. Make the following changes to the front-panel setup:

Set:	A SEC/DIV	2 μs
	CH 1 VOLTS/DIV	500 mV
	CH 2 VOLTS/DIV	2 V
	TRIGGER SLOPE	– (minus)
Select BANDWIDTH		
Set:	20 MHz	On
Select TRIGGER MODE		
Set:	AUTO	On

c. Connect the Full-Field Signal output of the video signal generator to the CH 1 input of the scope via a 75 Ω cable and a 75 Ω terminator.

d. Set the generator output for a field square wave producing a 100 IRE pedestal output for all lines. One line of video, with sync tip and color burst, should be displayed on screen in CH 1. (See top waveform in Figure 5-12.)

e. ADJUST—R419 while watching the output signal on the bench scope. First turn R419 all the way clockwise. Now, slowly rotate the adjustment counter-clockwise until the IRE pedestal appears on both the rising and falling edge of the waveform and the bottom of the waveform moves up slightly. Adjustment is correct when the output is not overdriven, with the IRE pedestal missing on the rising and edges, or underdriven, with excessive aberrations on the bottom of the waveform. (See bottom waveform in Figure 5-12.)

f. Disconnect the test setup. Perform, in reverse order, subparts b-f in part 3 of the Removal and Replacement procedure to return the processor board to its normal position.

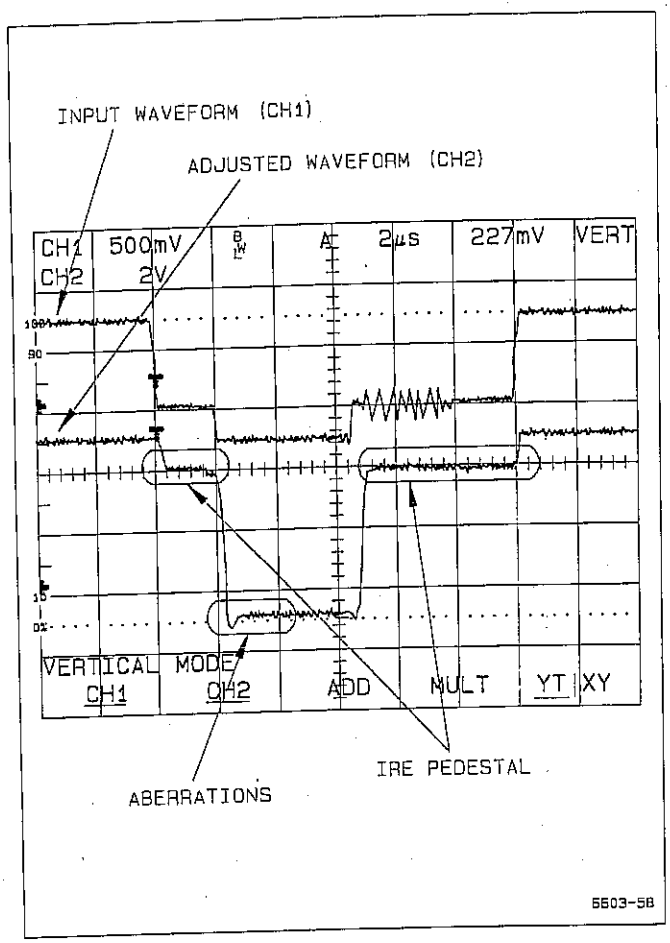


Figure 5.12 Input and output (after adjustment) waveforms.

SELF CALIBRATION

Equipment Required:

None

1. Self Calibration

a. Turn the instrument POWER ON and allow a 10 minute warm-up period. Note that the instrument's cabinet should be in place when performing this subsection of this procedure. (If an Internal Calibration was performed and J156 removed, do not reinstall J156 prior to reinstalling the cabinet unless an External Calibration is NOT to be performed after execution of a Self Calibration.)

b. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.

c. Press the menu button labeled CAL/DIAG (menu will change).

d. Press the menu button labeled SELF CAL. "RUNNING" will be displayed in the lower right corner of the crt screen for approximately 10 seconds as the instrument performs its automatic calibration routine.

NOTE

After successful completion of the automatic calibration routine, "RUNNING" will disappear from the CRT screen and "PASS" will be displayed above the SELF CAL menu button label. Press the MENU OFF/EXTENDED FUNCTIONS button to return the instrument to control settings in effect before the Self Calibration was initiated. If the automatic calibration routine is NOT successful (errors are detected), the EXTENDED DIAGNOSTICS menu will be displayed with accompanying error messages. Perform the following parts only if the instrument fails the Self Calibration; otherwise, Self Calibration has been completed.

e. Press the MENU OFF/EXTENDED FUNCTIONS button to turn off the EXTENDED DIAGNOSTICS menu.

f. Repeat parts b through d. If the instrument displays the EXTENDED DIAGNOSTICS menu again, refer the instrument to qualified personnel for servicing; otherwise, Self Calibration has been successfully completed.

EXTERNAL CALIBRATION

Equipment Required (see Table 4-1):

Calibration Generator (Item 3)

NOTE

J156 must be removed (see step 1, part a of Internal Adjustments) and a Self Calibration executed before this subsection can be performed. After performance (or partial performance) of this subsection, the cabinet should be removed and J156 reinstalled. Installation of this jumper will prevent inadvertent loss of the Calibration constants established by performance of this procedure. See the introduction of this procedure for further detail.

1. Attenuator Gain Adjustments.

a. Press the MENU OFF/EXTENDED FUNCTIONS button—twice, if a menu is presently displayed—to call up the Extended Functions menu.

b. Press the menu button labeled CAL/DIAG. (The menu will change.)

c. Press the menu button labeled EXT CAL to display the EXT CAL menu. Then press the menu button labeled ATTEN.

d. Set the Calibration Generator for a DC output. (See the generator Operators manual.)

NOTE

Do not attempt to calibrate CH 1 and CH 2 simultaneously via a dual-input coupler. The resulting reduction of the scope's input impedance can degrade the calibration-signal amplitude, leading to inaccurate calibration.

e. Connect the STD OUTPUT of the Calibration Generator to the CH 1 input connector through a 50-Ω cable.

f. Press the menu button that is labeled ATTEN GAIN. ("CONNECT CH1 TO 0.2VDC" will appear.) Set the generator output to 0.200 volts.

g. Press the ATTEN GAIN button again. ("RUNNING" will be displayed near the lower right corner of the screen.)

h. When the display changes from "CONNECT CH1 TO 0.2VDC" to "CONNECT CH1 TO 2.0VDC," change the generator output to 2.000 volts and press the ATTEN GAIN button.

i. When the display changes from "CONNECT CH1 TO 2.0VDC" to "CONNECT CH1 TO 20.VDC" change the generator output to 20.00 volts and press the ATTEN GAIN button.

j. When the display changes from "CONNECT CH1 TO 20.VDC" to "CONNECT CH2 TO 0.2VDC" disconnect the STD OUTPUT of the Calibration Generator from CH 1 and connect it to the CH 2 input connector.

k. Change the generator output to 0.2 volts and press the ATTEN GAIN button.

l. Repeat Steps h and i, substituting CH2 for CH1.

NOTE

When the sequence is finished, "RUNNING" will disappear from the CRT screen. If the calibration was successful, the ATTEN GAIN label will be marked "PASS." If the calibration was NOT successful, the label will be marked "FAIL." Perform Steps m and n only if the instrument fails the Attenuator Gain calibration sequence; otherwise, go to Step o.

m. Recheck the test setup and ensure that the Calibration Generator is set for a DC output. Reperform the Self Calibration subsection of this procedure.

n. Repeat parts a through i. If the instrument fails the Attenuator Gain Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, Attenuator Gain Calibration has successfully been completed.

o. Disconnect the test setup.

2. Channel Delay Adjustments.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice to display the Extended Functions menu. (Two presses are necessary if any menu is presently displayed, one press if no menu is displayed.)

b. Press the menu button labeled CAL/DIAG (menu will change).

c. Press the menu button labeled EXT CAL to display the EXT CAL menu. Then press the menu button labeled ATTEN.

d. Connect the FAST RISE OUTPUT of a Calibration Generator to the CH 1 and CH 2 input connectors through a 50-Ω cable, a 10X attenuator, and a dual input coupler.

e. Set the Calibration Generator for a FAST RISE output. (See the generator Operators manual).

f. Press the menu button that is labeled ATTEN GAIN. "CONNECT BOTH CHANNELS TO A FAST RISE SIGNAL VIA A TERMINATED COAX AND A DUAL INPUT CONNECTOR" will appear.) Set the generator output to MAX.

g. Press the RUN button. ("RUNNING" will be displayed near the lower right corner of the screen.)

NOTE

After successful completion of the Channel Delay Calibration sequence, "RUNNING" will disappear from the CRT screen and "PASS" will be displayed above the CHAN DLY menu button label. If the calibration routine is NOT successful, "FAIL" will be displayed above the CHAN DLY button label. Perform the following parts only if the instrument fails the Channel Delay Calibration sequence; otherwise, Channel Delay Calibration is complete.

h. Recheck the test setup and ensure that the Calibration Generator is set for a fast rise output. Reperform the Self Calibration subsection of this procedure.

i. Repeat parts a through g. If the instrument fails the Channel Delay Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, Channel Delay Calibration has successfully been completed.

j. Disconnect the test setup.

3. Trigger Adjustments.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.

b. Press the menu button labeled CAL/DIAG (menu will change).

c. Press the menu button labeled EXT CAL to display the EXT CAL menu.

d. Connect the STD OUTPUT of a Calibration Generator to the EXT TRIG 1 and EXT TRIG 2 input connectors through a 50 Ω cable and a dual input coupler.

e. Set the Calibration Generator for a DC output (see the generator Operators manual).

f. Press the menu button labeled TRIGGER ("CONNECT TRIGS TO GND" will be displayed) and set the generator output to 0.2 mV (~GND).

g. Press the TRIGGER button again ("RUNNING" will be displayed near the lower right corner of the screen).

h. When the display changes from "CONNECT ... TO GND" to "CONNECT ... TO 0.5V" change the generator output to 0.5 V and press the TRIGGER button.

i. When the display changes from "CONNECT ... TO 0.5V" to "CONNECT ... TO 2.0V" change the generator output to 2 V and press the TRIGGER button.

NOTE

After successful completion of the Trigger Calibration sequence, "RUNNING" will disappear from the CRT screen and "PASS" will be displayed above the TRIGGER menu button label. If the calibration routine is NOT successful, "FAIL" will be displayed above the TRIGGER button label. Perform the following parts only if the instrument fails the Trigger Calibration sequence; otherwise, Trigger Calibration is complete.

j. Recheck the test setup and ensure that the Calibration Generator is set for a DC output. Reperform the Self Calibration subsection of this procedure.

k. Repeat parts a through i. If the instrument fails the Trigger Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, Trigger Calibration has been successfully completed.

l. Disconnect the test setup.

4. Ramp (REPET) Calibration.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.

b. Press the menu button labeled CAL/DIAG (menu will change).

c. Press the menu button labeled EXT CAL to display the EXT CAL menu.

d. Press the menu button labeled REPET. The EXT CAL menu will display "RUNNING" momentarily and then display "PASS" or "FAIL." The calibration for REPET is then complete.

5. CTE Calibration.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice to display the Extended Functions menu. (Two presses are necessary if any menu is presently displayed, one press if no menu is displayed.)

b. Press the menu button labeled CAL/DIAG (menu will change).

c. Press the menu button labeled EXT CAL to display the EXT CAL menu. Then press the menu button labeled CTE CAL. A short-synopsis of the next calibration step will be displayed.

NOTE

The message "THIS MUST BE THE LAST STEP" also appears in the menu. It is a reminder that the CTE Calibration must be done after any adjustment of the CCD clocks or Transient response. (See steps 2 and 4 under "Internal Adjustments" in this section).

d. Connect the FAST RISE OUTPUT of a Calibration Generator to the CH 1 and CH 2 input connectors through a 50-Ω cable, a 5X attenuator, and a dual input coupler.

e. Set the Calibration Generator for a FAST RISE output at a 100 kHz frequency. Set the generator amplitude to maximum. (See the generator Operators manual as required).

f. Press the menu button that is labeled EXECUTE. ("RUNNING" will appear in the lower right corner as the calibration executes.)

NOTE

After successful completion of the CTE Calibration sequence, "RUNNING" will disappear from the CRT screen, the instrument will switch to the Extended Calibration menu, and "PASS" will be displayed above the CTE CAL menu button label. If the calibration routine is NOT successful, "FAIL" will be displayed above the CTE CAL button label. Perform the following parts only if the instrument fails the CTE Calibration sequence; otherwise, Channel Delay Calibration is complete.

g. Recheck the test setup and ensure that the Calibration Generator is set for a fast rise output. Reperform the Self Calibration subsection of this procedure.

h. Repeat parts a through f. If the instrument fails the CTE Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, CTE Calibration has successfully been completed.

i. Disconnect the test setup.